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Performance Analysis of Double Material Cylindrical Surrounding Gate MOSFET

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Abstract*— The investigation explored how self-heating and temperature sensitivity impact the linearity of a double-material cylindrical surrounding gate MOSFET. Results indicate that self-heating can reduce the device's linearity by decreasing transconductance and increasing output conductance. Temperature sensitivity affects the device's mobility and threshold voltage. Hence, it is essential to count on these factors during the planning and assessment of double-material cylindrical surrounding gate MOSFETs (DMCSG MOSFET) to guarantee peak performance. The study utilized a TCAD 3-D device simulator to obtain these results. The DMCSG MOSFET is an innovative transistor design that demonstrates improved performance characteristics compared to standard MOSFETs. This device utilizes a double material cylindrical gate surrounding the channel to enhance control and improve electrostatic integrity, resulting in better transistor performance. With its cylindrical gate structure enclosing the channel, the DMCSG MOSFET achieves superior gate control while minimizing short channel effects. By incorporating two different materials in the gate, it enhances electrostatic integrity, reducing gate leakage and improving device reliability. This transistor design also presents several advantages over traditional planar MOSFETs. The cylindrical gate geometry enables better electrostatic control, resulting in reduced power consumption and improved switching speed. Moreover, the DMCSG MOSFET demonstrates outstanding scalability, rendering it fitting for cutting-edge integrated circuit designs. Within this abstract, we provide a synopsis of the DMCSG MOSFET's pivotal characteristics, encompassing its dual-material surrounding gate configuration and enhanced electrostatic management. We emphasize its benefits over traditional MOSFETs, such as diminished power consumption, heightened switching speed, and augmented scalability. The DMCSG MOSFET shows great potential for use in high-performance electronic devices and integrated circuits, paving the way for advancements in the field of semiconductor technology.

***Keywords*—DMCSG, MOSFET, TCAD, short channel effect**

I. INTRODUCTION

Continuous downscaling of semiconductor devices has been significantly influenced by advancements in device fabrication technology and channel engineering. However, as MOSFET dimensions are aggressively scaled down, the gate's ability to control the channel region diminishes due to increased Short Channel Effects (SCEs) [1]. To address this challenge, semiconductor engineers have investigated and developed novel device structures to further improve device performance by mitigating SCEs [2]. In this context, junctionless MOSFET structures have emerged as a promising candidate for reducing SCEs and improving scalability.A Surrounding Gate MOSFET (SG-MOSFET) is a type of MOSFET that has a gate electrode that surrounds the semiconductor channel, which helps to expand the device's electrical performance [3]. The gate configuration enables more effective control of the electric field within the channel, resulting in reduced leakage current and enhanced device reliability. SG-MOSFETs have possible applications in like low-power electronics and biosensors.

This investigation centers on examining the influence of self-heating and temperature fluctuations on the linearity of a double-material cylindrical surrounding gate MOSFET[4].A Cylindrical Surrounding Gate MOSFET (CSG MOSFET) is a form of MOSFET that has a cylindrical gate structure surrounding a vertical channel. It is also known as a vertical surround-gate MOSFET or vertical gate-all-around MOSFET. The CSG MOSFET is a three-terminal device with a source, drain & gate terminal. The gate electrode is formed around the vertical channel and is isolated electrically from it through a thin oxide layer. The gate may be either p-type or n-type, and the channel is usually made of a highly-doped n-type material. The gate structure enfolds the channel, which enables excellent electrostatic control of the channel and the ability to scale the device to very small dimensions [5].

Self-heating and temperature sensitivity can significantly impact the linearity of a double-material cylindrical surrounding gate MOSFET (DMC-SG MOSFET) in the different manner. Self-heating occurs when the power dissipated within the MOSFET increases its temperature. This can influence the linearity of the device . Increased temperature can cause a shift in the threshold voltage of the MOSFET, which affects the transconductance and, consequently, the linearity. Higher temperatures typically reduce carrier mobility due to increased phonon scattering [6]. This reduction in mobility can lead to decreased drain current and affect the linearity. The subthreshold slope may degrade with increasing temperature, impacting the subthreshold conduction characteristics and thus the linearity. Excessive self-heating can lead to thermal runaway conditions, where the device temperature increases uncontrollably, severely impacting linearity and potentially leading to device failure. Temperature sensitivity refers to how changes in ambient temperature affect the device performance. Key parameters like threshold voltage, mobility, and saturation velocity are temperature-dependent. Variations in these parameters with temperature can cause non-linearities in the MOSFET's I-V characteristics. Increased temperature generally results in higher leakage currents due to enhanced carrier generation-recombination rates, impacting the linearity at lower current levels. In a double-material gate structure, temperature variations can cause differential thermal expansion of the materials, potentially leading to mechanical stress and variations in gate control effectiveness. Temperature variations can affect DIBL, altering the short-channel effects and impacting linearity [7].

Impacts on Linearity

- Distortion: Non-linearities in the I-V characteristics due to self-heating and temperature sensitivity can introduce harmonic distortion, which is detrimental to analog and RF applications.
- Gain Compression: As the temperature increases, the gain of the MOSFET can decrease due to reduced carrier mobility and threshold voltage shifts, leading to gain compression.
- Intermodulation Distortion: Temperature-induced variations can also affect the intermodulation distortion performance of the device, which is crucial for high-frequency applications.

The anticipated outcomes of this endeavor include:

- Examining the influence of self-heating and temperature sensitivity on the linearity of a double-material cylindrical surrounding gate MOSFET.
- Investigating the improvement in on-current (Ion) attributed to the High K dielectric positioned over the channel.

The performance and reliability of a Double Material Cylindrical Surrounding Gate MOSFET (DMCSG MOSFET) can be significantly affected by the internal heat generation. Self-heating is the result of power dissipation within the device, which causes a temperature increase, thereby impacting its characteristics. Within DMCSG MOSFETs, self-heating can be attributed to the high current density within the device, leading to temperature increases in the gate and channel regions. This, in turn, can reduce the mobility of charge carriers, resulting in increased resistance and decreased device performance. Device designers have at their disposal various techniques to address the effects of self-heating. These methods include optimizing the structure and material properties of the device, adjusting its geometry, and implementing thermal management schemes [8]. These strategies offer improved electrostatic control over the channel and reduce parasitic capacitance, thereby enhancing the performance of the device. He use of high-K (high dielectric constant) materials instead of traditional SiO_2 oxides has been shown to mitigate self-heating effects (SHE) in MOSFETs and enhance device performance. This approach leverages the superior thermal and electrical properties of high-K materials to address issues associated with aggressive downscaling of device dimensions.

High-K Materials for Improved Thermal and Electrical Performance High-k materials such as ZrO_2, HfO_2, La_2O_3, and Al_2O_3 have demonstrated a significant reduction in device temperature, which mitigates the self-heating effects. These materials possess better thermal conductivity and lower thermal resistance compared to SiO_2, leading to enhanced heat dissipation and reduced junction temperatures [9]. The use of high-K dielectric materials also reduces gate tunneling currents. This is because high-K dielectrics allow for thicker gate oxides without compromising the gate capacitance, thereby reducing leakage currents and improving device reliability [10].

1) *On-State Current (I_{on})*

A higher on-state current indicates better conductivity and higher drive current capability, which improves the transconductance. Higher gm leads to better amplification and linearity. High Ionreduces the channel resistance, leading to a more linear relationship between the gate voltage and the drain current, minimizing distortions. A high Ion contributes to a lower output conductance s), which is essential for maintaining linearity in the saturation region. This results in a more constant drain current for varying drain voltages), reducing output non-linearity [11]. Better on-state performance enhances the control of the gate over the channel, leading to a more uniform electric field distribution and reduced short-channel effects (SCEs), which improve linearity.

2) *Off-State Current (I_{off})*

Lower off-state current indicates reduced leakage currents, which is crucial for maintaining high linearity [12]. Leakage currents can introduce noise and reduce the signal integrity, leading to non-linear behavior. A lower I_{off} improves the subthreshold slope, enhancing the transition between off and on states. This sharp transition is critical for maintaining linearity at low signal levels. Minimizing I_{off} helps in reducing DIBL, which improves the threshold voltage stability. Stable threshold voltage ensures that the device operates linearly across different operating conditions and voltages. Reduced off-state currents lead to better electrostatic integrity, where the gate exerts more effective control over the channel, resulting in improved linearity by reducing variations in the threshold voltage [13].

Both high Ion and low Ioff contribute to a stable threshold voltage. A stable threshold voltage ensures that the device switches more predictably and linearly, enhancing overall linearity. Improved on-state and off-state currents reduce harmonic distortion, which is critical for analog and RF applications. Lower harmonic distortion means the output signal more accurately follows the input signal[14].Better control of on-state and off-state currents also reduces intermodulation distortion, where multiple signal frequencies mix, resulting in undesired output frequencies.

Utilizing high-k dielectrics, as mentioned earlier, can improve gate control and reduce leakage currents, enhancing both Ion and Ioff.Implementing optimized doping profiles and advanced channel materials (e.g., strained silicon, SiGe) can further enhance the on-state performance and reduce off-state leakage. MOSFET with dual-material gates improves electrostatic control, as the different work functions help modulate the channel potential more effectively, reducing SCEs and improving linearity [15]. Incorporating self-heating management techniques ensures that thermal effects do not degrade I_{on} and I_{off}, maintaining device performance and linearity. Improving the on-state current and reducing the off-state current are crucial for enhancing the linearity of double-material cylindrical surrounding gate MOSFETs. These improvements lead to better transconductance, reduced channel resistance, minimized leakage currents, stable threshold voltage, and overall reduced non-linear distortions. Through material innovations, advanced device designs, and effective thermal management, the linearity of DMC-SG MOSFETs can be significantly improved, making them more suitable for high-performance analog and RF applications.

II. METHODOLOGY

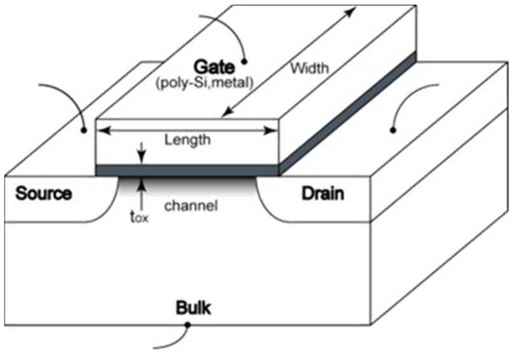

Fig. 1: MOSFET schematic view [2]

schematic representation of a surface channel MOSFET demonstrates the physical gate length: Figure 1 illustrates a surface-channel MOSFET, where the gate sits on top of the device and the channel is positioned directly below the gate. The gate is separated from the channel by a thin insulating layer typically made of silicon dioxide (SiO2). In the schematic view of a surface channel MOSFET, one would observe the source and drain regions at opposite ends of the device, with the gate situated in the middle. The gate is visualized as a slim line atop the device, isolated from the channel by the insulating layer. In contrast, the gate width refers to the dimension perpendicular to the physical gate length. The physical length of the gate is an important parameter in MOSFET design, as it affects the device's electrical characteristics, for instance, the threshold voltage and saturation current. The gate length is typically scaled-down as technology advances, to increase device performance and density. However, as the gate length decreases, it becomes increasingly difficult to maintain control over the channel, and several short-channel effects, like DIBL and hot carrier effects, become more significant.

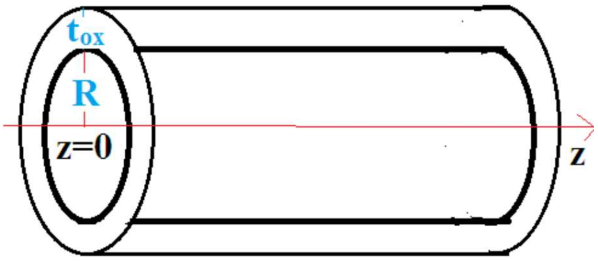

Fig. 2: Channel region with gate oxide CSG MOSFET [2]

Variance (Figure 2 illustrates a cylindrical surrounding gate MOSFET, a type of metal-oxide-field-effect transistor featuring a gate surrounding the channel region in a cylindrical structure. This MOSFET variant is also known as a Fin FET or a 3D transistor, given its gate structure's three-dimensional form. The channel region in a cylindrical surrounding gate MOSFET is commonly constructed from semiconductor material like silicon and is coated with a thin layer of gate oxide. This gate oxide acts as an insulating barrier between the gate and the channel, with its thickness being crucial for optimal device performance.

The gate of a cylindrical surrounding gate MOSFET typically consists of a conductive material, such as doped polysilicon, and encircles the channel region in a cylindrical fashion. In the DMCSG MOSFET, this gate is isolated from the channel by the gate oxide. This design attribute offers improved control over the channel in comparison to a planar MOSFET, delivering enhanced electrostatic regulation of the channel [16, 17].

III. SIMULATION RESULTS

Due to their enhanced performance and scalability, cylindrical surrounding gate MOSFETs are widely utilized in modern semiconductor technology. They offer better control of the channel, reduced power consumption, and improved switching speed compared to planar MOSFETs. Simulating the cylindrical surrounding gate MOSFET using a 3-d device simulator in TCAD.

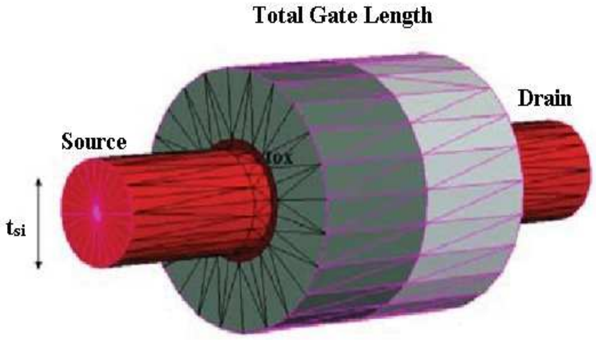

Fig. 3: Device-structure-of-DMCSG MOSFET

Figure 3 shows DMCSG MOSFET device structure - a type of MOSFET that has a gate surrounding the channel region in the form of a cylindrical structure, but with a unique design in which the channel and gate are made of different materials. This configuration leads to enhanced device performance and lowered power consumption when contrasted with traditional MOSFETs. The device structure of a DMCSG MOSFET typically includes the following materials:

- Substrate: Typically, a silicon substrate forms the bottom layer of the device, although alternative materials may also be utilized.
- Channel: To enhance the device's performance, the channel region commonly consists of a high-mobility semiconductor material like germanium.
- Gate oxide**:** Providing insulation between the channel and the gate, a thin layer of gate oxide is deposited on the channel.
- Inner gate: Made of a low-work function metal such as aluminium, the inner gate of the DMCSG MOSFET wraps around the channel in a cylindrical shape.
- Spacer oxide: A layer of spacer oxide is applied over the inner gate, serving as insulation between the outer and inner gates.
- Outer gate: Wrapped around the spacer oxide layer in a cylindrical shape, the outer gate is composed of a high-work function metal like titanium nitride.
- Source and drain regions: These heavily doped regions are located on either side of the channel region, typically consisting of the same material as the channel.

The dual-material design of the DMCSG MOSFET allows to improve the device's on-state current, while the outer gate made of a high-work function metal helps in downgrading off-state leakage current. Additionally, the use of a high-mobility channel material helps to further improve device performance.

IV. DEVICE STRUCTURE & SIMULATION SETUP

Figure 1(a) and Figure 1(b) provide a 2D view of HKG-DP-DCSG and HKG-DM-DCSG MOSFETs, respectively, which are extracted using TCAD. By the 2D cutaway depiction, SiO2 and HfO2are used as thin covers of cylindrical channels. The parameters of the simulation are enlisted in Table 1.DD model has been employed for the transport of carriers. Mobility simulations have utilized several models. This simulation-based analysis does not take into account Quantum confinement effects (QCEs) .

TABLE I. DIMENSIONS OF $HKG - DM - DCSG, HKG - DP - DCSG\ MOSFET$ FOR SIMULATION

Parameters	HKG – DM – DCSG MOSFET	HKG – DP – DCSG MOSFET
Channel length(L)	30 nm	
Source/Drain Doping (Ns, Nd)	10^{20} /cm^3	
Channel Doping (NA)	10^{15} /cm^3	
Thickness of the oxide (tox)	1 nm	
High K Thickness (Hf02)	1 nm	
Thickness of the channel (tsi)	10 nm	
Dielectric Bag length (DBL)	-	5 nm
Dielectric Bag thickness (DBT)	4.9eV	4.79eV

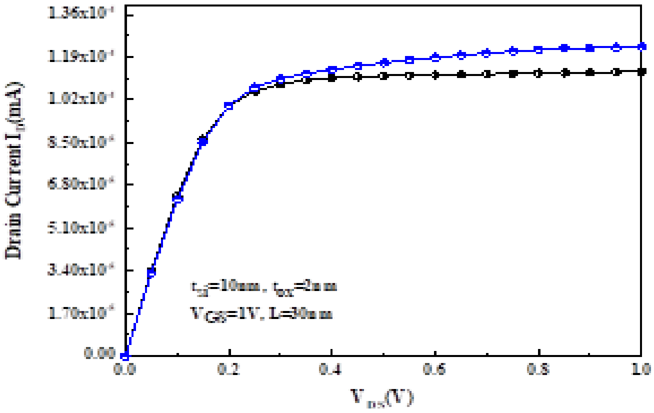

Fig.4**:** Input characteristic (I_D) and V_{DS} between CSG & CDSG MOSFET

TABLE II. I_{ON} AND I_{OFF} VS TEMPERATURE FOR CSDG MOSFET

S.No.	Temperature (K)	I_{ON} (mA)	I_{OFF} (mA)
1.	250	1.18×10^{-4}	0.2×10^{-10}
2.	275	1.17×10^{-4}	0.3×10^{-10}
3.	300	1.16×10^{-4}	0.3×10^{-10}
4.	325	1.13×10^{-4}	0.4×10^{-10}
5.	350	1.10×10^{-4}	0.4×10^{-10}
6.	375	1.08×10^{-4}	0.9×10^{-10}
7.	400	1.05×10^{-4}	1.6×10^{-10}

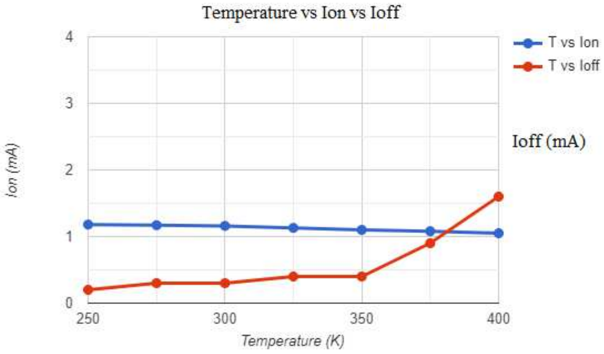

Fig.5: I_{ON} and I_{OFF} vs Temperature for CSDG MOSFET

Figure 5 shows the variations of I_{on} and I_{off} at different temperatures as indicated in the graph. The trends of both Ion and I_{off} follow a similar pattern for the devices under examination. Rising temperature leads to an increase in off current due to the concentration of minority carriers, and it also causes a degradation of on current due to the mobility of majority carriers. As a result, I_{off} increases while Ion decreases with temperature elevation.

In Figure 6, the transconductance is shown as the temperature is increased from 250K to 400K.

TABLE III. I_{ON} AND I_{OFF} VS TEMPERATURE FOR CSDG MOSFET

S.No.	Temperature (K)	Transconductance (g_m)
Parameters: t_{si}=10nm, t_{ox}=2nm, V_{DS} =1 V, L=30nm		
1.	250	3.31×10^{-4}
2.	275	3.10×10^{-4}
3.	300	2.90×10^{-4}
4.	325	2.85×10^{-4}
5.	350	2.60×10^{-4}
6.	375	2.58×10^{-4}
7.	400	2.52×10^{-4}

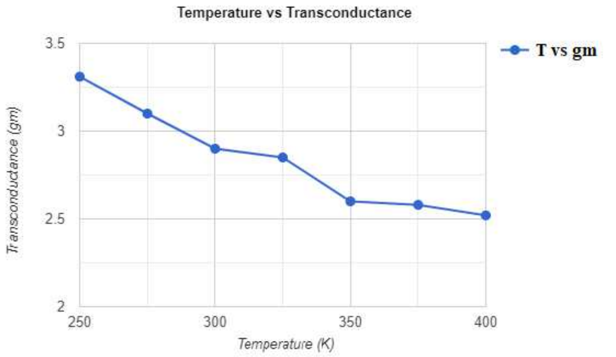

Fig 6. Transconductance vs Temperature

V. CONCLUSION

This investigation explores the effects of self-heating through the evaluation of the operational performance of High K Gate-DM-DCSG and HKGate-Dual pocket-DCSG MOSFETs across a temperature range from 250K to 400K. The results of this analysis are then presented and discussed. Various electrical constraints have been assessed for both devices across the specified temperature range. The HKG-DP-DCSG MOSFET demonstrates a higher resistance to Self-Heating Effects (SHEs) when compared to the High-K G-Dual Material -DCSG MOSFET across the entire temperature spectrum. In contrast to the other devices under investigation, the HKG-Dual Pocket-DCSG MOSFET exhibits a higher value of Ion while simultaneously showing a lower value of Ioff. Based on these observations, it can be concluded that devices fabricated with DP offer superior performance compared to those produced with DM and are less susceptible to temperature variations.

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