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Implementing Blockchain Technology for Enhanced Privacy and Security in Federated Learning Healthcare Models	253
<i>Huthaifa Ayad Al-Ani, Ruya yilmaz saber, Nada Sami Naser, Mouhamd Hashim, Ghaith Ayad Kadhem, Heba A. Abd-Alsalam Alsalam, and Tarun Goma</i>	
Asymptotic Outage Analysis with Diversity: A Journey Over the Family of $\kappa - \mu$ /Shadowed Fading	267
<i>Ankit Jain, Imran Ullah Khan, Puspraj Singh Chauhan, Vimal Bhatia, and Rahul Maurya</i>	
Energy Aware Solutions Based on Swarm Intelligence for Secure Digital Healthcare Systems	278
<i>Ahmed Zkear Abass, Ahmed Ali Ibrahim, Ali Abdul Razaq, Ghaith Ayad Kadhem, Mouhamd Hashim, Heba A. Abd-Alsalam Alsalam, and Mohammed Ahmed Mustafa</i>	
Laguerre Quadrature Polynomial Approximation for SEP Analysis in Extended η - μ Fading Distributions	293
<i>Manish Kumar Dixit, Arun Kumar Singh, and Saurabh Dixit</i>	
Chronic Kidney Disease Prediction Using Machine Learning	304
<i>T. Neetha, Manoranjan Dash, A. Mallikarjuna Reddy, K. Harshitha, M. Sai Surya, and Shashidar</i>	
Spacer Dielectric Engineering for Enhanced Analog/RF Performance in Dual-Metal Double Gate GaAs/Si _{1-x} Ge _x TFETs	313
<i>Rohit Tripathi, Vedvrat, Syed Hasan Saeed, and Vivek Kumar</i>	
Design and Analysis of Nanosheet FET-Based Memory Architectures for Future Technology Nodes	323
<i>Abhishek Kumar, Tarun Chaudhary, Balwinder Raj, and Anit Srivastava</i>	
Reliability Analysis of Ge-Pocket Non-uniform Vertical TFET	332
<i>Rajeev Kumar Sachan, Vedvrat, Hasin Alam, Abhai Shankar Chaurasia, and Sushroot</i>	
Improving Interpretability and Performance with Knowledge Guided Self Supervised Vision Transformers for Lung and Heart Segmentation	344
<i>Tarik Khairallah Alasadi, Mahmood Anees Ahmed, Hameed H. Khalaf, Salwan Asaad Dawod, Heba A. Abd-Alsalam Alsalam, Rusul Adnan Dawood, and Preeti Sharma Nair</i>	



Spacer Dielectric Engineering for Enhanced Analog/RF Performance in Dual-Metal Double Gate GaAs/Si_{1-x}Ge_x TFETs

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Abstract. The present study provides an investigation DMDG GaAs/Si_{1-x}Ge_x tunnel field-effect transistor device (TFET) with dielectric spacer based on its analog and RF performance metrics. The device performance is assessed for varying spacer dielectric medium ($\epsilon_r = 1, 3.9, 7.5, 9, 25$). For precise device modeling and electrostatic control, all simulations are conducted using the 2D TCAD simulation platform. The study reveals that by using the high- k spacers the device parameters i.e., transconductance, cut-off frequency, and gain bandwidth product, substantially increased whereas the threshold voltage decreased. However, use of low- k spacers suppresses the parasitic capacitances but lowers ON-state current (I_{ON}). The incorporated spacer modulation indicates that $\epsilon_r = 9$ offers an optimized device DC and RF characteristic and obtains a higher I_{ON}/I_{OFF} ratio. These findings emphasize the significance of dielectric spacer selection as a significant design element for energy-efficient and high-speed nanoelectronic circuits.

Keywords: Spacer dielectric geometry · Hetero-dielectric spacer · Dual-Metal Double Gate (DMDG) · GaAs/SiGe TFET · Analog/RF performance · Fringing field control · RF Figures of merit (FOM) · Energy-efficient nanoelectronics

1 Introduction

TFETs have arisen as viable substitutes for conventional MOSFETs due to their sub-threshold swing (SS) performance beneath the thermionic threshold of 60 mV/dec and their enhanced energy efficiency in ultra-low-power applications [1–3]. TFETs employ BTBT as the principal conduction mechanism, leading to sharp switching characteristics and diminished leakage currents, rendering them appealing for logic and analog/RF applications. To augment tunneling probability and electrostatic control, device architectures employing heterojunctions [4, 5], Work-function engineered [6–8]; high- k /low- k double-gate stack configurations [9] have been thoroughly investigated. While previous study has predominantly emphasized gate stack engineering [10], source-pocket optimization [11–15], and material selection [16], there has been comparatively scant