Dissertation

on

Performance Evaluation of Fully Depleted Silicon on Insulator MOSFET

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MASTER OF TECHNOLOGY

in

Electronic Circuits and Systems

Submitted By:

Yogendra Kumar Sharma

(1900103914)

Under the Guidance of

Dr. Imran Ullah Khan

Department of Electronics & Communication Engineering.

INTEGRAL UNIVERSITY, LUCKNOW

May-2022

UNDERTAKING FROM THE CANDIDATE

This is to certify that I, Yogendra Kumar Sharma, have completed the M.Tech Dissertation work on the topic **“Performance Evaluation of Fully Depleted Silicon on Insulator MOSFET”** under the supervision of Dr. Imran Ullah Khan for the partial fulfillment of the requirement for the Master of Technology (M.Tech.) in Electronic Circuits and Systems from Department of Electronics and Communication Engineering, Integral University, Lucknow. This is an original piece of work &I have not submitted it earlier elsewhere.

Date: 14/05/2022

Place: Lucknow

Signature

Yogendra Kumar Sharma

Enrollment No.: 1900103914

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I, Yogendra Kumar Sharma, certify that the work embodied in this Dissertation is my own bonafide work carried out by me under the supervision of Dr. Imran Ullah Khan at Integral University, Lucknow. The matter embodied in this Dissertation has not been submitted elsewhere for the award of any other degree/diploma. I declare that I have not willfully lifted up some other's work, para, text, data, results, etc. reported in the journals, books, magazines, reports, dissertations, thesis, etc., or available at web-sites.

Date: 14/05/2022

Place: Lucknow

Signature

Yogendra Kumar Sharma

Enrollment No.: 1900103914

CERTIFICATE FROM THE SUPERVISOR

This is to certify that **Yogendra Kumar Sharma** has carried out the research work presented in the dissertation entitled **“Performance Evaluation of Fully Depleted Silicon on Insulator MOSFET”** for the award of Master of Technology (M.Tech.) in Electronic Circuits and Systems from Department of Electronics and Communication Engineering, Integral University, Lucknow under my supervision. To the best of my knowledge, the contents of this dissertation have not been submitted to any other institute or university for the award of any degree.

Signature of Supervisor

Full Name: Dr. Imran Ullah Khan

Designation: Associate Professor (L-II)

Address: Deptt. of ECE, Integral University

Date: 14/05/2022

Place: Lucknow

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"He is the source of all light and his light is diffused throughout the universe God has given the man intelligent speech, power of expression and capacity to understand clearly the relations of things." First and foremost I would thank the Almighty whose infinite grace make all things possible.

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We are living in the age of electronics and this field has witnessed radical changes over the last decades. I have observed vast application of electronics in almost every walk of life. The lot of work are being done in the field of Fabrication and Micro Electronics Technology. This fascinated me to do something in this field as a student of Electronics Engg.

In my project work many people have contributed time and efforts in bringing the project to a conclusion. I feel great pleasure in expressing my sense of gratitude and sincere thanks to my project guide **Dr. Imran Ullah Khan**, Department of Electronics and Communication Engineering for his consistent and careful guidance throughout this project work, I feel proud to get the opportunity to work under him which has enlightened my thoughts and enriched my experience. I am grateful to **Dr. Syed Hasan Saeed**, Professor and Head, Department of Electronics and Communication Engineering for providing necessary facilities in the department. I am also thankful to **Dr. Shailendra Kumar** for his constant support throughout this semester.

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Date: 14/05/2022
Place: Lucknow

Signature
Yogendra Kumar Sharma
Enrollment No.: 1900103914

ABSTRACT

Now days, the development of VLSI technology is mainly directed toward the miniaturization of semiconductor devices which in turns is heavily depend on the advancement in the complementary metal oxide semiconductor technology. Silicon-on-Insulator technology has been receiving a lot of alternation owing to capacitance, shorter channel length, body biasing and faster switching transistor, limited variability and faster running transistor.

Silicon on Insulator is bringing interesting new possibilities compared to conventional bulk technology. A slowing of the rate of the progress in CMOS technology has highlighted recently. The extra performance offered by fully depleted silicon on insulator. Performance improvements concern the power consumption and the communication speed. The silicon on insulator technology may cut the power consumption nearly by half with speed improvements close to 40%.

The thesis presents a systematic study of silicon on insulator based nano metal oxide semiconductor field effect transistor using Atlas module of SILVACO software. A 20 nm silicon on insulator MOSFET is virtually fabricated using Atlas. Aluminum, N. poly, W (Tungsten), and WSi_2 (Tungsten Silicide) are used as the gate metals and respective characteristics are obtained and compared. Finally WSi_2 was used as final gate metal since it provides required band offset that result in positive threshold voltage without any additional implant in channel region. Other parameters like the variation of I_D vs. V_{GS} characteristics at different values are obtained. Also variation of drain current as function of drain to source voltage is being observed.

TABLE OF CONTENT

S. No.	Topics	Page No.
	List of Figure	viii
	List of Table	ix
	List of Abbreviations	x
1	**CHAPTER 1**	1-9
1.1	Introduction	2
1.2	Silicon on Insulator Metal Oxide Semiconductor Field Effect Transistor	2-4
1.3	Fully Depleted SOI MOSFETs	5
1.4	MOSFET Scaling	5-6
1.5	Need of Silicon On Insulator	6-8
1.6	Report Organization	9
2	**CHAPTER 2**	10-19
2.1	Literature survey	11-19
3	**CHAPTER 3**	20-33
3.1	Fully depleted (FD) vs Partially depleted (PD)	21
3.1.1	Comparison between partially depleted (PD) and fully depleted (FD) SOI MOSFETs	22-24
3.2	Silicon On Insulator Characteristics	24-27
3.3	No Latch Up	27-28
3.4	Methodology	28
3.4.1	SILVACO ATLAS	28-29
3.4.2	Commands Atlas	29
3.5	Structure specification	29-32
3.6	Designing of Nano based FDSOI MOSFET	32-33
4	**CHAPTER 4**	34-37
4.1	Metal Selection	35-36
4.2	I_D versus V_{GS} Characteristics	36
4.3	Variation of I_D as Function of V_{DS}	37

5 **CHAPTER 5** 38-39
5.1 Conclusion 39
5.1 Future Scope 39

REFERENCES 40-43

LIST OF FIGURES

Figure No.	Title	Page No.
1.1(a)	Idealized geometry of the SoI MOSFET	3
1.1(b)	SoI MOSFET structure	3
1.2	Partially Depleted and Fully depleted SOIMOSFET	4
1.3	Cross sectional of MOSFET	4
1.4	Fully depleted SOI MOSFETs	5
1.5	Effect of Channel Length Modulation	7
1.6	SOI Wafer	8
3.1	Structure of (a) Fully Depleted and (b) Partially Depleted SOI MOSFET	21
3.2	Drain Junction Capacitance of SOI MOSFET	25
3.3	Latch-up in CMOS	27
3.4	Meshing of Semiconductor Device	30
3.5	Complete structure of 20 nm SOI MOSFET	33
4.1	I_D-V_{GS} curves for different metal N. poly, Aluminum, W (Tungsten), and WSi_2 (Tungsten Silicide)	35
4.2	I_D vs. V_{GS} curves	36
4.3	I_D vs. V_{DS} curves	37

LIST OF TABLE

Table No.	Name of Table	Page No.
1.1	Improvement in technology Node over the years	6
3.1	ATLAS command groups with primary statements in each group	29
4.1	Simulated threshold voltages of different gate metals	36

LIST OF ABBREVIATION

Abbreviation	**Name**
I_D	Drain Current
V_{DS}	Drain to source Voltage
V_{GS}	Gate to source Voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
SiO_2	Silicon Dioxide
SoI	Silicon-on-Insulator
W	Tungsten
WSi_2	Tungsten Silicide
Al	Aluminium
EOT	Effective Oxide Thickness
Å	Angstrom
TCAD	Technology Computer Aided Design

CHAPTER 1

INTRODUCTION

1.1 Introduction

VLSI system implement Silicon complementary Metal Oxide Semiconductor (CMOS), is the leading technology [1]. However, there exist inherent parasitic couplings between devices and the substrate in CMOS. Due to these two reasons it gives rise to a range of problems in circuit applications. These include high parasitic capacitance, latch up and short channel effects. As the technology gets advances the minimum feature length has been shrinking continuously, which results in a prominent increase in these problems. Though these problems cannot be eliminated completely but some special processing techniques and designs have been introduced to migrate these problems. To improve the performance of the devices circuits and systems, the use of Silicon-on-insulator has been introduced in 1970s in CMOS technology. However the SoI CMOS technology has become more commonly available due to the recent breakthrough in material fabrication, such as separation by implementation of Oxygen (SIMOX) [1] and Band-and-Etch-back SoI (BE SoI) [2]. There are some tremendous benefits of SoI which includes simplified process, enhanced performance and increased integration density. CMOS based SoI microchips offer a 30% reduction in power consumption and a 30% improvement in speed. Also, a two year performance gain over an equivalent bulk CMOS technology can be achieved [1]. For the future generations of VLSI systems SoI CMOS is likely to become the dominant technology.

The semiconductor industry has showed an exponential growth in the number of transistors per integrated circuit for several years. This is actually a result of Moore's law prediction. The evolution of electronics, information technology (IT), and communication is due to continuous progress of silicon based CMOS technology. This continuous progress is achieved by the scaling of its dimensions. To improve both device density and performance, CMOS scaling is the main driving force of Silicon technology advancement.

1.2 Silicon on Insulator Metal Oxide Semiconductor Field Effect Transistor

Silicon on Insulator (SoI) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a sort of structures, a semiconductor layer for instance, germanium, silicon is shaped over a protector layer which might be a covered oxide layer framed on a semiconductor substrate.

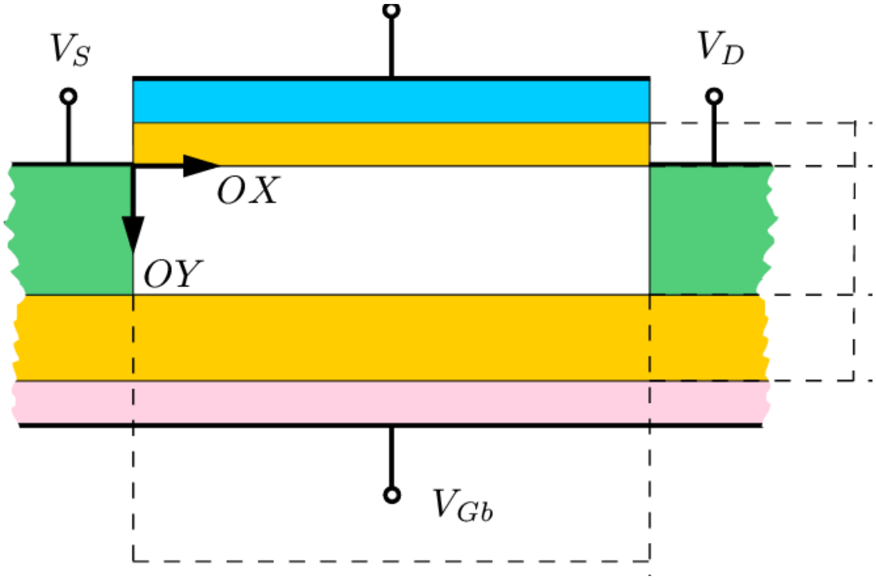

Figure 1.1(a): Idealized geometry of the SoI MOSFET [1]

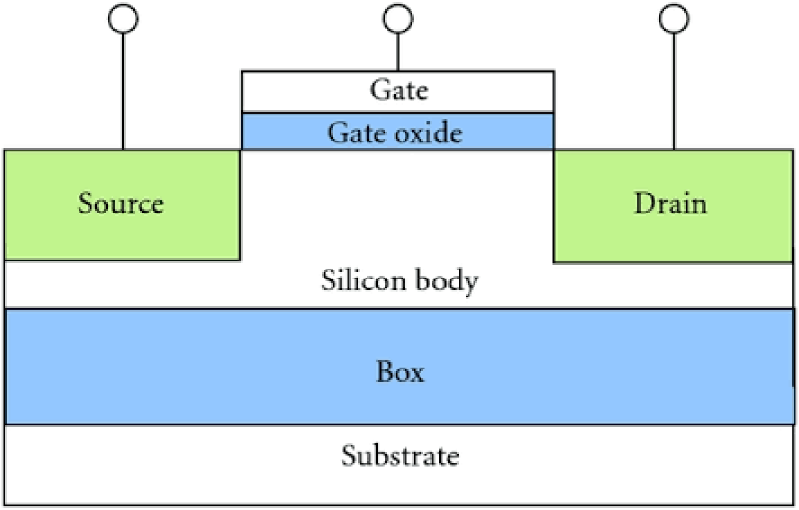

Figure 1.1 (b): SoI MOSFET structure [1]

There are two kinds of silicon on encasing MOSFET

1. Partially Depleted (PD) SoI MOSFET
2. Fully Depleted (FD) SoI MOSFET

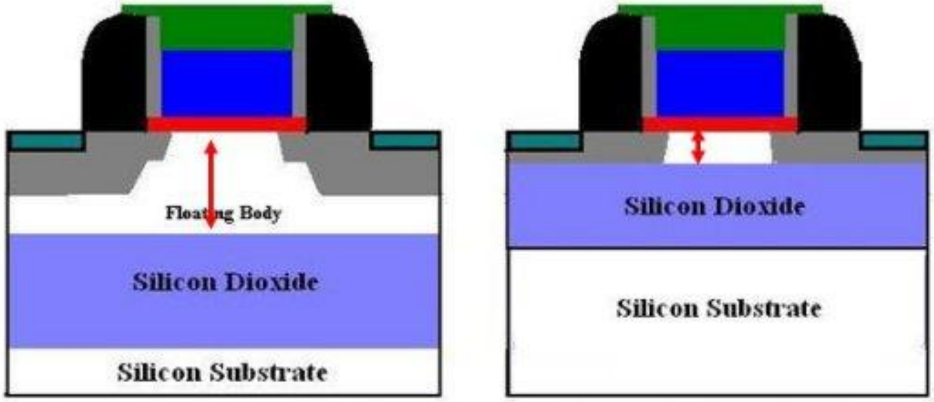

Figure 1.2: Partially Depleted and Fully depleted SOIMOSFET [2]

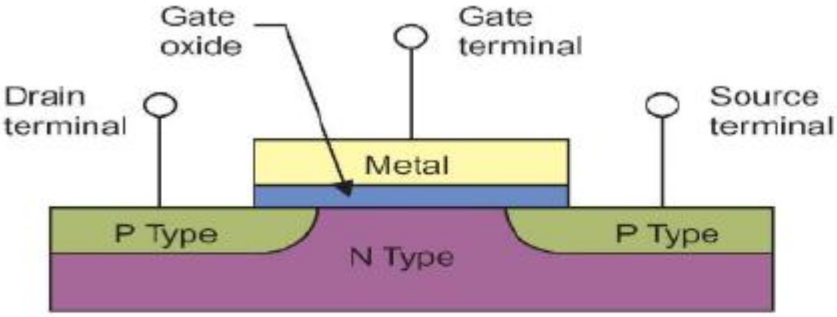

Figure 1.3: Cross sectional of MOSFET [2]

The fundamental device conditions of PD SOI MOSFETs are the same concerning mass devices, with the exception of obviously from the intricacies emerging from the drifting body (FBE).

1.3 Fully Depleted SOI MOSFETs

In FDSOI case, the front and back channels are electro-statically coupled during device operation. This electrostatic coupling makes the front channel FD SOI parameters subject to the back gate Voltage, including channel current, edge voltage, sub-limit incline and so on.

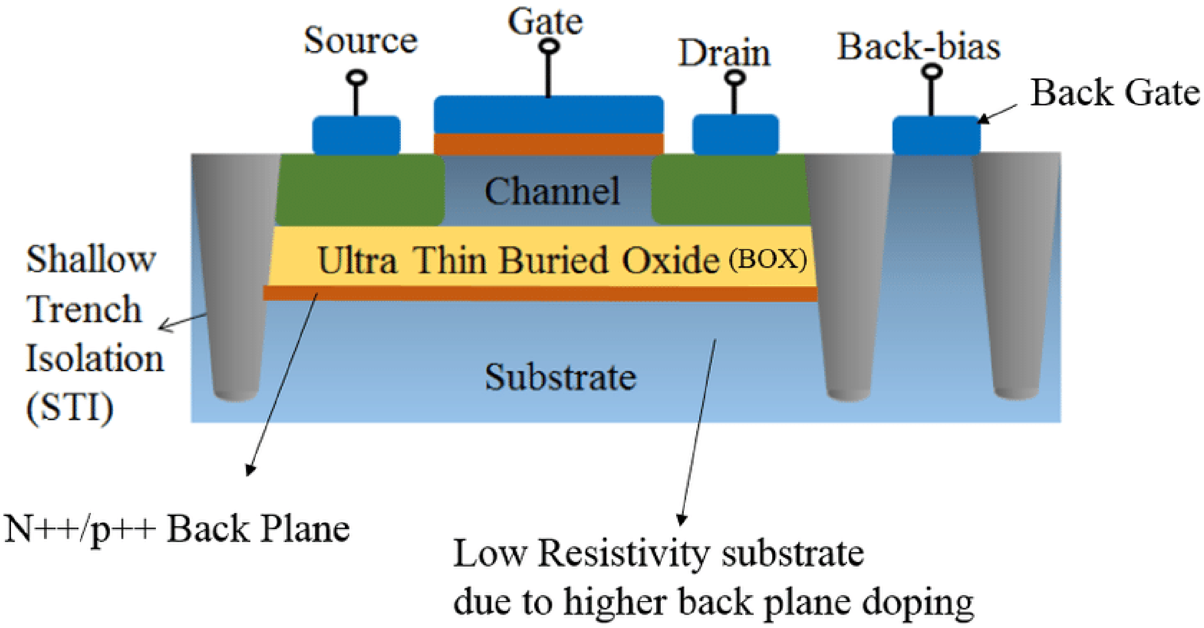

Figure 1.4: Fully depleted SOI MOSFET [3]

1.4 MOSFET Scaling

Miniaturization of MOSFETs is highly implant and desirable for several reasons. The very first and most important reasons is make transistors smaller in size is to integrate more and more number of devices in a given chip area. The result is that the chip has more function in the same area. The cost per integrated circuits is basically related to the number of chips that can be produced per wafer. Hence with the reduction of the size of ICs allow more chips per wafer and it reduces the price per chip. Once a new technology is introduced, the number of transistors per chip has been doubled every 23 years over the past 30 years. For example the number of MOSFETs in a microprocessor fabricated in a 45nm technology will be twice. This doubling of the transistor is firstly observed by Gordon Moore in 1965 [3] This is known as Moore's law. Due to some reasons smaller transistors switch faster. For example, size can be reduced with the scaling of MOSFET. It requires all dimensions of the device to reduce proportionally. Channel length, channel width, and oxide thickness are the main dimensions of the device. When these factors are scaled down by that factor while transistors channel resistance remains the same.

Since 1965 to till now, the price of one bit semiconductor has been dropped 100 million times. The main and foremost reason in the increment of electronics is "miniaturization". The circuit becomes smaller by the reduction in the size of the transistors and interconnects. As a result, more circuits can be fabricated on each silicon wafer. These have been an improvement in speed and power consumption in speed and power consumption in ICs.

Moore's Law

In the year 1965, Gordon Moore made a tremendous and vital observation according to which in every 18 or 24 months or so the number of devices on a chip gets doubled. Moore's law shows a continuous miniaturization. A new technology node is introduced or a new technology generation is introduced with the reduction of minimum line width. Some of the examples of the technology generation or technology node is shown in table 1.1. In the above table the numbers shows the minimum metal line width. Poly-Si length may be even smaller. All the features in circuits layout, such as the contact holes are reduced in size to 70% of previous node.

Table 1.1: Improvement in technology Node over the years]

Year	2004	2006	2008	2010	2011	2013	2016	2022
Technology Node	90nm	65nm	45nm	32nm	22nm	16nm	14nm	10nm

1.5 Need of Silicon On Insulator

To build better digital devices and enhances the user experience the size of transistors must be reduced while increasing performance and reducing power consumption. As the transistor shrinks, the length of the gate is reduced. The control that exercises over the channel region is also reduced, lowering the transistors performance. Some unwanted leakage current flows even when the transistor is switched off. In order to minimize this leakage current while continuing to deliver a high performance bulk Silicon transistor have beware ever more complex adding additional levels of manufacturing complexity at an ever increasing rate. In technology smaller 20nm new solution need to found to reduced complexity while bringing the benefits of reduced silicon geometry that the industry expect. SoI FET is an approach that delivers these benefits while enabling simplification of the manufacturing process. Unlike SOI some other technology doesn’t change the fundamental geometry of the transistor.

Shorter Channel Length

The SOI transistor has the shorter effective channel as compared to bulk Si Simplification. The shorter channel reduces the time necessary for the electron flow from source to drain leading to a faster transistor. In order to improve the transistor performance a voltage can be applied to the substrate this method is body biasing facilitates the creation of the channel between the source and drain which result in faster switching transistor.

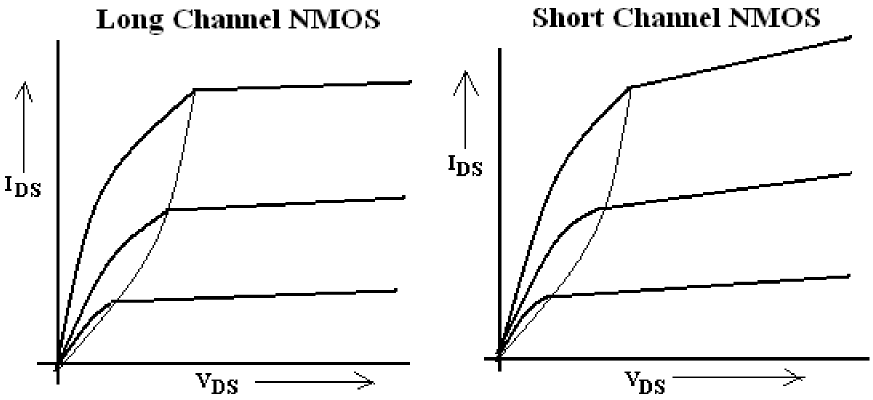

Figure 1.5: Effect of Channel Length Modulation [5]

Body Biasing and Faster Switching Transistor

The biasing creates a buried gate below the channel making the SOI act like a vertical double gate transistor. In bulk technology the ability to do body biasing is very limited due to parasitic current leakage. The buried gate in the SOI transistor prevents any leakage in the substrate. This allows a much higher voltage on the body leading to a significant boost in the performance. In a chip there are billions of transistors characteristics of each transistor are not exactly because the different quantities of dopants injected into the channel during the manufacturing process is the same.

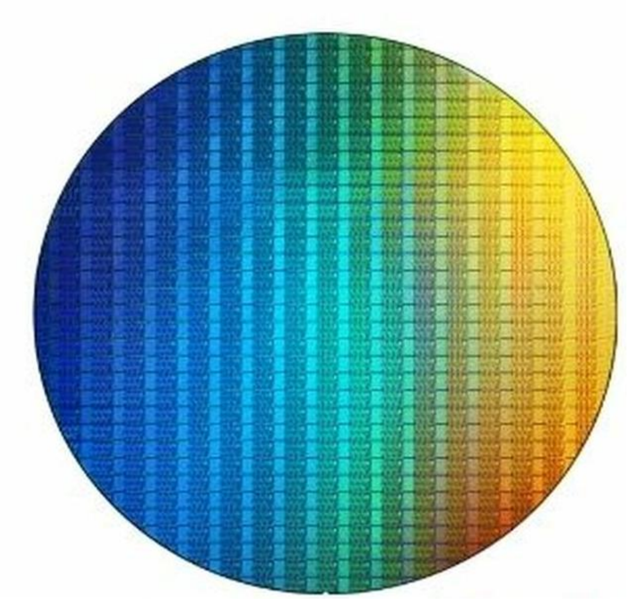

Figure 1.6: SOI Wafer [6]

In SOI, dopants usage is greatly reduced thereby limiting the variability results characteristics of each transistor is closely to average in the process. This allows transistor runs faster for a given voltage. SOI chip is able to operate at lower voltage than delivers the same performance. SOI attractive with lower power consumption.

1.6 REPORT ORGANIZATION

The report has been divided into five chapters as below:

Chapter 1 includes introduction of metal oxide semiconductor field effect transistor, silicon on insulator, its type and need.

Chapter 2 is literature survey of some related research.

Chapter 3 deals with methodology and fully depleted silicon on insulator metal oxide semiconductor field effect transistor characteristics.

Chapter 4 represents overall results and discussions.

Chapter 5 conclusion and future scope

CHAPTER 2

LITERATURE SURVEY

Literature Survey

Silicon-on-Insulator or SOI is an inventive innovation that use the set up planar process while guaranteeing a continuation of the productivity enhancements anticipated by Moore's law. SOI conveys the pass on measure decreases, control decreases, increments in execution and expanded usefulness anticipated by Moore's Law without the need to present drastically more mind boggling producing forms. This enables planners and makers to make the really creative, get through items that can make new markets or overwhelm built up ones. FD-SOI is the response to the frequently clashing necessities that test fashioners of low power hardware gear.

Ranka, D. et al. [1] fully depleted (FD) silicon on insulator (SoI) metal oxide field effect transistor (MOSFET) is the leading contender for sub 65nm regime. this paper presents a study of effects of work functions of metal gate on the performance of fully depleted silicon on insulator metal oxide field effect transistor. sentaurus tcad simulation tool is used to investigate the effect of work function of gates on the performance fd-soi mosfet. specific channel length of the device that had been concentrated is 25nm. from simulation we observed that by changing the work function of the metal gates of fd-soi mosfet we can change the threshold voltage. hence by using this technique we can set the appropriate threshold voltage of fd-soi mosfet at same voltage and we can decrease the leakage current, gate tunnelling current and short channel effects and increase drive current. Silicon technologies have progressed faster year to year. The main issue must be concentrate about silicon technologies is effects of reducing the dimension of devices. The scaling down of devices is strongly required to achieve high integration density and better device performance. Due to reduction in the channel length the short channel effects and leakage current become important issue that degrades the device performance in terms of leakage current and short channel effects. To overcome the problem, a new circuit design techniques has been introduce for a newer technologies such as Silicon-on-Insulator (SOI). SOI refers to placing a thin layer of silicon on top of an insulator, usually silicon dioxide ($SiO2$) or known as buried oxide layer (BOX). MOSFETs fabricated on SOI substrate that having a relatively thin SOI layer is known as fully depleted SOI and for thick SOI layer is known as partially depleted SOI. Usually, for fully-depleted SOI devices, the thickness of silicon is about less than bulk depletion width. The full isolation in SOI device provide many advantages such as the drain-to substrate capacitance can be neglected due to insulator (SiO2) that having dielectric constant lower than Silicon. In recent years, silicon-on insulator (SOI) has attracted considerable attention as a potential alternative substrate for low power application. The most common approach for reducing the power is power supply scaling.

Malviya, A.K.et al. [2] work focused on improving the on current and reducing the off current with the use of different types of the high-k spacer. Some spacers provide better on current and some provide lower off current (leakage current). Lowering of leakage current can also be controlled by use of high-K BOX (buried oxide layer). In this paper, Tio2, Hfo2, Si3N4 and Sio2 at 50 nm gate length is used. Modified Source dual material gate fully depleted silicon on insulator structure. All simulation part has been done on Silvaco tool. By looking at ITRS roadmap it can comprehend how much device scaling has been done and with the help of Moore's low, we can foresee the upcoming node technologies. Because of day by day scaling in the channel length, short channel effects (SCEs) like DIBL, GIBL, hot electron effect, Off-state leakage current, threshold voltage roll-off come into the picture. For proper operation of MOSFET current should be controlled properly and current is controlled by voltage. For better control over current, gate voltage should have good control over the channel. It is possible only when there is no SCEs like DIBL (Drain induced barrier lowering). To overcome these problems SOI technology came into the picture. Silicon on insulator (SOI) CMOS technology helped us a lot in improving the Off-state leakage currents and short channel effects. As we reduce the size of the device, the width of dielectric become a critical feature. Due to scaling below 65nm fringing electric filed to become a more important factor for short channel effect. Using high-k materials we can get less series resistance because of the fringing electric field and it kicks in the good On-state driving current. Some papers have a good idea to overcome with the SCEs. Ming-Wen Ma et al. discussed the effect of high-k dielectrics on 65-nm length SOI device. Paper
provides an idea of using the high-k spacer proposed modeling of FDSOI on the Vth of with the sidewall oxide spacer structure. Introduced a new way to tackle the problems. Vimal et al. described MS FDSOI in detail. Sandeep et al. explained different device parameters variation

with work function. By looking over these papers we tried to replace the gate oxide with two different dielectrics in symmetric and asymmetric manner. This paper, have used 50 nm gate length MS DMG FDSOI device. It helped in improving the On-state and Off-State current ratio in comparison to previous MS DMG FDSOI.

Flandre, D. et al. [3] described that fully depleted (FD) silicon-on-insulator (SOI) innovation offers remarkable open gates in the field of low-voltage, low-control CMOS circuits. Next to the notable decrease of parasitic capacitances because of dielectric segregation, FD SOI MOSFETs in reality display close perfect body factor, subthreshold slant and current drive. These benefits are both hypothetically and tentatively researched. Unique circuit considers at that point indicate how an essential FD SOI CMOS process takes into consideration the blended manufacture and activity under low supply voltage of simple, computerized and microwave parts with properties significantly better than those got on mass CMOS. The benefits of completely drained SOI CMOS innovation, devices and circuits for the acknowledgment of low-voltage low-control circuits essentially beating mass CMOS executions. The outcomes exhibit that an essential ease CMOS process on SIMOX substrates with symmetrical limit voltages around 0.33V takes into consideration the blended manufacture and activity under a supply voltage of 1.2V, of: ± advanced parts with upgraded speed and static and dynamic power execution; ± simple segments with improved speed, exactness, power, swing and commotion execution; ± and microwave segments with improved gain and recurrence execution over mass partners.

Vandana, B. et al. [4] the fundamental circuit issues of the mass and SOI innovation, and furthermore demonstrates the predominant highlights of SOI which incorporate the procedure and creating circuits. Lastly, end demonstrates the correlation of two innovations by giving the proper plan portrayal. It additionally demonstrates the concise depiction of the CMOS Bulk innovation and SOI innovation that are contrasted and one another. In the wake of concentrate the different circuit issues of both the innovations. SOI gives the predominant outcomes than Bulk innovation, which builds the circuit exhibitions, high unwavering quality, expels the parasitic capacitance, punch through issue and the circuit conservativeness. Henceforth SOI innovation is the main and up and coming innovation in both miniaturized scale and nano hardware. With the presentation of Silicon-on-Insulator MOSFET, the gadget innovation has seen the scaling from several micrometer to many nanometer. It has experienced various fruitful auxiliary adjustments and still is in research to reintroduce it into sub 10nm time. In the work the recessed source/deplete structure is being investigated down to 10nm channel length. The surface potential, edge voltage and subthreshold normal for short-channel FD Re-S/D UTB SOI MOSFETs have been displayed utilizing Evanescent mode examination. Displaying of substrate incited surface potential impacts for the gadget was completed and was incorporated into the gadget model to enhance the exactness of gadget attributes. It is discovered that at low channel doping back surface of the channel overwhelms the present stream while at higher channel doping front surface of the channel ends up prevailing. Additionally it was discovered that the SISP impact is overwhelming in reversal area of the substrate while in aggregation locale it tends to be ignored. The investigation of SCE with channel thickness, entryway oxide thickness and recessed-S/D profundity were completed to enhance the gadget execution. The gadget demonstrating results were plotted with the ATLAS reenactment up to 20nm channel length and model outcomes were observed to be in superb concurrence with ATLAS reenactment. In light of the accomplishment of the model for Re-S/D SOI MOSFET, its execution up to 10nm what's more, beneath can be tried utilizing quantum repression recreation in ATLAS likewise the execution advancement can be done to find the future extent of the gadget. Scaling of the transistor has been colossal effective at the outset with decrease of the door oxide thickness and increment of doping focus. Moving into littler measurement, those are insufficient to beat the short channel impact. Beginning with changing in materials and pursued by gadget design is required which require completely exhaustion task. This article surveys the completely consumption task of thin assortment of silicon on protector of cutting edge MOSFETs.

Alok Kumar Kushwaha described that the mass Si MOSFET has been the primary device shaping the foundation of the improvement of ultra-high thickness ICs. Be that as it may, because of persistent scaling down, a circumstance has achieved, where the execution parameters of the MOSFETs are corrupted (due to the essential physical cutoff points), to the degree that it is exceptionally hard to manufacture ICs with nano-scale mass MOSFETs.

Another age device, which can offer great execution parameters i.e. low power utilization and fast, notwithstanding for nano-sacle devices, is required. Distinctive gate structures alongside SOI wafer innovation are presently seen as the most critical rising designing innovation for use in driving edge CMOS IC generation amid the following 3-5 years. One conceivable situation amid this period is the quick reception of SOI wafers instead of single gem silicon wafers currently utilized as beginning substrates for top-of-the-line rationale device (e.g., microchips) and SOC (System On Chip) applications at the 0.13 and 0.10 micron innovation hubs. SOI innovation appear to offer an amazing stage for coordinating RF and advanced circuits on a similar chip due to its prevalent RF/rapid execution. Silicon-On-lnsulator (SOI) CMOS innovation is a potential innovation for future VLSI framework executions. Inferable from finish dielectric detachment, SOI innovation offers predominant MOS devices with stifled CMOS hook up, higher pressing thickness and higher speed.

M. K Mohd Arshad et al. [5] explanation has begun with correlation among mass and silicon-on-cover, at that point we feature the principle parameter in thin body SOI controlling the short channel impacts. From that point onward, we present the advanced and RF figures of merit in thin body SOIMOSFETs. The primary favorable circumstances of thin body SOI MOSFETs are the back-door biasing either from the substrate of halter kilter double gate. These configurations are not achievable in other technologies, for example, FinFET. Despite the fact that the thin SOI gadget is better since its downsides are to a great extent dominated by its significant focal points, the decision is as yet amazing since SOI beginning material is more costly than mass Si as it requires additional handling ventures to fabricate. This represents an obstruction to the determination by industry in spite of the fact that SOI brings more benefits. Be that as it may, as the gadget door length contracts down, it is trusted the thin body SOI gadget offers better choice in the future.

Rahou, F. Z. et al. [6] has explained the qualities of completely drained double metal door silicon on separator is considered and introduced, the outcome is contrasted and that of single material door MOSFET the outcome shows that short channel impact decreases in double material door MOSFET. Moreover the electrical attributes of MOSFET can be controlled by door length and work work designing. So this work demonstrates better execution of double material entryway with contrast with that of single material door silicon on separator. Double material door MOSFET is proposed to diminish the short divert impact In a solitary material entryway as per the recreation result MOSFET with various work in the door give better power over the channel and reductions the short channel impact And additionally the outcomes demonstrated that double material door MOSFET has littler trans conductance and higher deplete conductance contrasted with that of single material door. Likewise the reenactment results demonstrate that the ideal proportion of L_1 and L_2 is solidarity, and ideal work distinction is equivalent to 0.4 ev for a completely exhausted double material door MOSFET.

Fatimah, A.H et al. [7] suggested simulation work is to compare the performance of gate all around nanowire and DG MOSFET and then study the effect of physical parameter on electrical behavior for both devices. The result of the simulated model of gate all around nanowire is compared with published data. It was found that when the gate length of double gate was scaled from 80nm to 10nm, the subthreshold slope is increasing from 62mV/dec to 162.7mV/dec. While for GAA, the subthreshold slope is increasing from 65.8mV/dec to 127mV/dec. The threshold voltage in double gate and gate all around at length of 80nm are 0.40646V and -0.17505V respectively. Even though heavy doping was good for suppressing short channel effect the lower doping concentration is desirable as the double gate and gate all around nanowire had higher on-state currents with 1.42×10^{-3}A and 3.23×10^{-4}A respectively. It also showed that the threshold voltage of double gate and gate all around nanowire increase from -0.0734V to 0.2312V and -0.0319V to 0.2232V respectively when the channel doping is varies from lower to higher concentration.

Islam M.J. et al. [8] used the cylindrical gate-all-around (CGAA) FET (field-effect transistor) structure with Indium Arsenide (InAs) nanowire is used as channel instead of silicon nanowire, and aluminium oxide is used as the gate dielectrics instead of silicon dioxide. The performance of this setup was demonstrated using ATLAS simulator of Silvaco TCAD software. Indium Arsenide is chosen due to its high electron velocity, high saturation velocity and low contact resistance, whereas, aluminium oxide is chosen because of its higher permittivity.

Simulation results indicate that the proposed combination is superior to the CGAA structures having channel-gate dielectrics that use combinations of silicon-silicon dioxide and Indium Arsenide-silicon dioxide. The effects of variation of nanowire radius, channel length and oxide thickness on the output and transfer characteristics curves, and also on the performance parameters such as maximum drain current, maximum transconductance, on resistance and inverse subthreshold slope are investigated to show the superiority of the proposed structure.

Pal A. et al. [9] extend the use of a 2D analytical model for the Dual Material Surrounding Gate MOSFET (DMSG) by solving the Poisson equation has been proposed and verified using ATLAS TCAD device simulator. Analytical modeling of parameters like threshold voltage, surface potential and Electric field distribution is developed using parabolic approximation method. A comparative study of the SCEs for DMSG and SMSG device structures of same dimensions has been carried out. Result reveals that DMSG MOSFET provides higher efficacy to prevent short-channel effects (SCEs) as compared to a conventional SMSG MOSFET due to the presence of the perceivable step in the surface potential profile which effectively screen the drain potential variation in the source side of the channel. A nice agreement between the results obtained from the model and the results obtained from numerical TCAD device simulator provides the validity and correctness of the developed model.

K. Han et al. [10] have proposed a novel Core–Insulator Gate-All-Around nanowire has been proposed, investigated, and simulated comprehensively and systematically based on 3 dimensional numerical simulation. Comparisons are carried out between gate all around and CIGAA. The new CIGAA structure exhibits low off-state current compares to that of GAA, making it a suitable candidate of future low-power and energy-efficient devices. The device performance of our proposed CIGAA nanowire using 3D TCAD simulation. Due to CIGAA’s lowered off-state current enabled by Core–Insulator, it shows high on-state current, low off-state current, low subthreshold swing, and high switching ratio. CIGAA has the potential to be used to fabricate low-power systems. Thus, the CIGAA nanowire is a promising candidate to extend CMOS scaling roadmap and future low power CMOS devices.

Sano et al. [11] developed a rigorous numerical model for threshold voltage (V_{th}) that includes a dependence on the back gate bias. A general steady state analysis of charge coupling between the front and back gate that yielded closed form expressions for V_{th} under all possible steady state charge conditions was presented. They also discussed the dependence of the linear region channel conductance on the back gate bias and other device parameters. Both *n*-type and *p*-type *SOI MOSFET* structures were considered. They analyzed the effect of the interface parameters on the back and the front threshold voltages. The temperature dependence of the threshold voltage of the ultra thin *SOI n*-channel *MOSFET*. The threshold voltage variation with temperature is significantly smaller in fully depleted devices than in bulk devices. In this paper, the dependence of V_{th} on the depletion level was also discussed.

Chen L. et al. [12] the statistical variation of V_{th} resulting from the randomness in impurity distribution in both bulk and SOI MOSFET was discussed. Their study revealed that the thresholdvoltage of DG FD SOI MOSFET is less sensitive to inherent fluctuations in impurity distribution and discussed the design considerations for minimizing the statistical variation in V_{th}. Over the past thirty years, the primary challenge for the IC designers has been the integration of an ever increasing number of devices with high yield and reliability.

However, as the device dimensions approach deep submicron regime, the characteristics of a conventional MOSFET approach that of a resistor. Increasing the threshold voltage through increased channel doping solves this difficulty. However, this would require higher supply voltage and also result in higher capacitance. This combination would result in higher power dissipation and low speed which are undesirable. So a tradeoff is required.

Yan et al. [13] has proposed the guidelines for the design of SOI MOSFETs. They discussed several structural variations of conventional SOI structure in terms of natural length scale to guide the design. The requirement of low voltage operation made the investigations of subthreshold characterization important. The subthreshold behavior of a MOSFET is characterized by the subthreshold swing, which has to be small enough to ensure low leakage current and sufficient overdrive necessary for high speed. The dependence of the subthreshold swing (**S**-factor)[*] on current capability of the MOSFET has been discussed for the gate length down to 0.1 µm. In the subthreshold region, the floating body (of FD SOI device) leads to a shift in the subthreshold slope which is smaller than the theoretical value of 60 mV / decade predicted for an ideal MOS transistor at room temperature.

Davis et al. [14] observed subthreshold slope as small as 50 mV / decade for n-channel MOSFETs fabricated on SOI substrate. Advances in SOI wafer technology have improved the material quality substantially leading to n-channel MOSFET subthreshold slope of less than 20 mV / decade. Good understanding of this subthreshold behavior of floating body SOI MOSFET is necessary for proper transistor design and circuit modeling. Previously reported **S**-factor models are based on one-dimensional analysis of the SOI MOSFET and cannot be applied to short channel devices where the potential distribution is essentially two dimensional. Two-dimensional analysis of subthreshold behavior using numerical analysis approach has been reported in for DG FD SOI devices.

Matloubian et al. [15] showed that n-channel SOI MOSFETs with floating bodies show a threshold voltage shift and improvement in subthreshold slope at higher drain biases.
This improvement was supported by the positive feedback between the body potential and the transistor channel current. Subthreshold slopes in submicron n-channel fully depleted silicon on insulator MOSFETs have been measured as a function of substrate bias and temperature as well as drain bias. It was found that for low drain voltage, a simple capacitor model could explain the experimental results. For large drain voltages anomalously sharp subthreshold characteristics was observed for large negative substrate biases. They also proposed a qualitative model based on the charge state of the lower SOI interface to explain the dependence of the anomalous effect on substrate bias. The model for current-voltage characteristics in subthreshold region for sub micrometer fully- depleted SOI-MOSFET. The above slope is computed for I_D vs V_G curve in subthreshold region with V_{DS} kept asconstant.

CHAPTER 3

METHODOLOGY and FDSOI MOSFET CHARACTERISTICS

3.1 Fully depleted (FD) vs Partially depleted (PD)

In PD MOSFET, a piece of the body locale remains undepleted or impartial while in FD MOSFET, entire of the body, the depletion area stretches out straight up to the body and BOX interface.

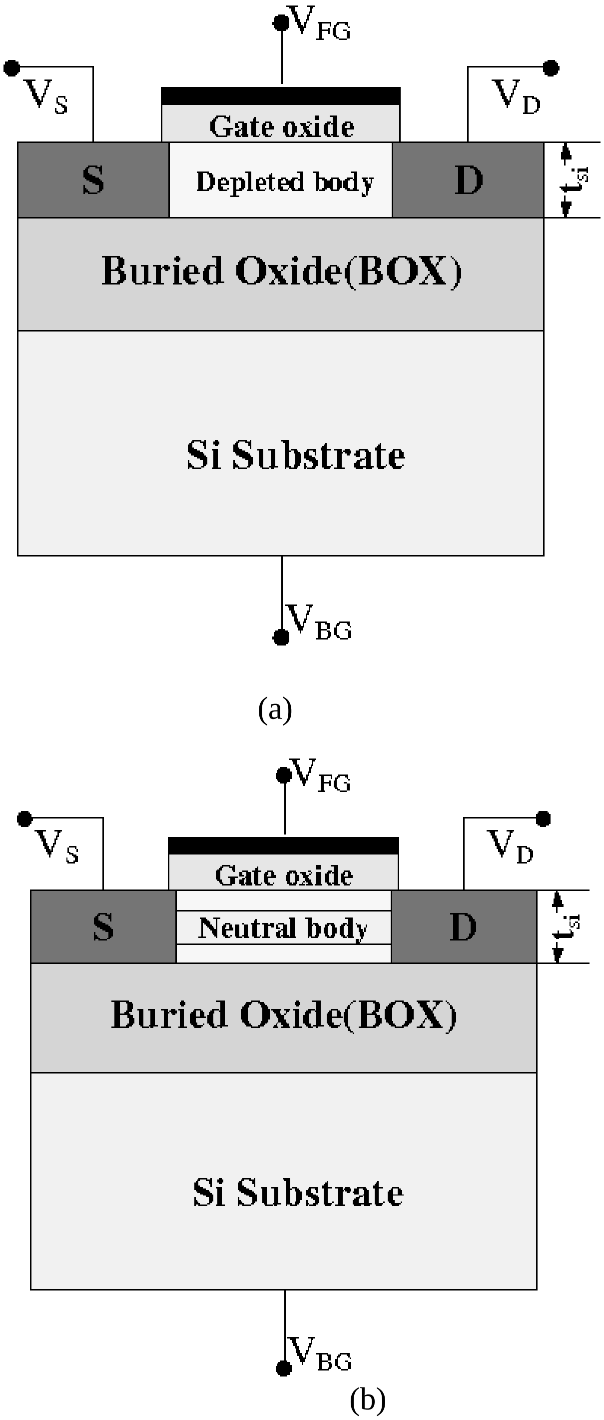

Figure 3.1: Structure of (a) Fully Depleted and (b) Partially Depleted SOI MOSFET

3.1.1 Comparison between partially depleted (PD) and fully depleted (FD) SOI MOSFETs

The attributes of FD and PD MOSFETs vary in the accompanying regards.

Subthreshold Slant

A vital component of FD SOI MOSFET is that they have soak subthreshold conduct describes by subthreshold swing near 60 mV/decade which is constraining an incentive for MOSFETs. The subthreshold conduct of PD SOI is like mass Si MOSFETs. Therefore, subthreshold attributes of FD SOI MOSFETs are unrivaled.

Kink in the Deplete Current Attributes

In PD SOI MOSFETs, a crimp (sharp ascent in deplete current at a specific deplete voltage) is seen in the I_D versus V_{DS} qualities as the deplete voltage is expanded for a settled gate voltage. As in n-channel. MOSFETs as the electrons stream towards the deplete they increase dynamic vitality and create electron-gap matches by affect ionization. The gaps so produced moves towards the source. In PD SOI device there is higher potential hindrance to the openings so the gap tend to gather in the body area in this manner expanding the body voltage. This causes edge voltage to drop, deplete current to build prompting significantly higher effect ionization. At the same time hindrance tallness for gaps likewise diminishes allowing more number of openings to achieve the source in this manner expanding the deplete current. This outcomes in sharp increment in the deplete current (a crimp) at some deplete voltage. To evade this crimp the collection of PD SOI MOSFETs should be associated with ground. In FD SOI devices, the potential obstruction to the opening at the source end is little since entire of the body district is exhausted of the transporters. In this way, there is no aggregation of openings in the body district and subsequent crimp in the deplete qualities.

Parasitic Bipolar Impacts

In FD SOI MOSFET, a parasitic bipolar transistor is shaped where source, body and deplete go about as producer, base and gatherer separately of parasitic transistor. In this transistor, base current is comprise of larger part transporters, created by affect ionization. Since the body locale is more drained in FD than PD SOI device. The parasitic transistor is more powerful in FD SOI devices. This transistor prompts a decrease to breakdown voltage between the source and deplete, littler edge voltage and strangely soak subthreshold conduct. This parasitic impact may likewise prompt single transistor hook wonder [21-23]. The parasitic bipolar impact can be smothered by stifling the age of dominant part bearer by affect ionization, diminishing the infusion proficiency of the parasitic bipolar transistor and by bringing down the vehicle productivity in the base of the transistor.

Dynamic Skimming Body Impacts

As said over, the SOI devices are completely segregated and their body potential isn't steady. The impacts of various body potential are all in all known as gliding body impact. Dynamic body coasting impacts allude to the device conduct when it is working in a circuit. The body potential changes due to affect ionization in larger part redistribution in the body locale when gate and deplete switch among high and low levels. FD SOI devices are steady and generally unaffected by the dynamic body impacts. Conversely the PD SOI devices are altogether touchy to dynamic body impact and require the body to be associated with a steady potential. These skimming body impacts have been known to cause the transient marvel in the entrance transistor of DRAMs and SRAMs that can prompt loss of charge in memory cell [23-25].

Impact of Self heating

Self-heating impacts are regular to both PD and FD SOI devices. The BOX layer which prompts better normal for the device is moreover in charge of its poor heat conduct. The oxide has a heat conductivity which is two requests of extent littler than that of silicon. Along these lines, the heat created by the deplete current can't escape through the BOX layer and must be disseminated by the interconnections by means of the contact of source, deplete and gate. This may results in increment in channel temperature and subsequent debasement device conduct.

3.2 Silicon On Insulator Characteristics

The SOI MOSFET characteristics are recorded below [22-31]

- Low deplete intersection capacitance: A schematic of cross-sectional perspective of SOI MOSFET at the deplete intersection is appeared in figure 2.2. The deplete intersection capacitance contains vertical intersection capacitance between the deplete and substrate (CVJ), the sidelong intersection capacitance (CLJ) between the side mass of the deplete and the body. The part (CVJ) is an arrangement blend of the capacitance of the covered oxide (CVJB) and the capacitance (CVJD) of the consumption area in the substrate underneath the BOX. All these capacitances are appeared in figure 2.2. Thickness of the body district is ordinarily not exactly 0.1 µm, so the capacitance (CLJ) is little. The vertical capacitances being in arrangement coming about still littler capacitance. Because of the above factor, generally deplete intersection capacitance in SOI MOSFET is substantially littler than the same in mass MOSFET. Commonly, the deplete intersection capacitance for a SOI MOSFET is bring down by one request of greatness as contrasted with the same in mass silicon MOSFET, having same contamination focus in the body. Because of lower deplete intersection capacitance; the power scattering amid the exchanging of the transistor is less in SOI MOSFETs.

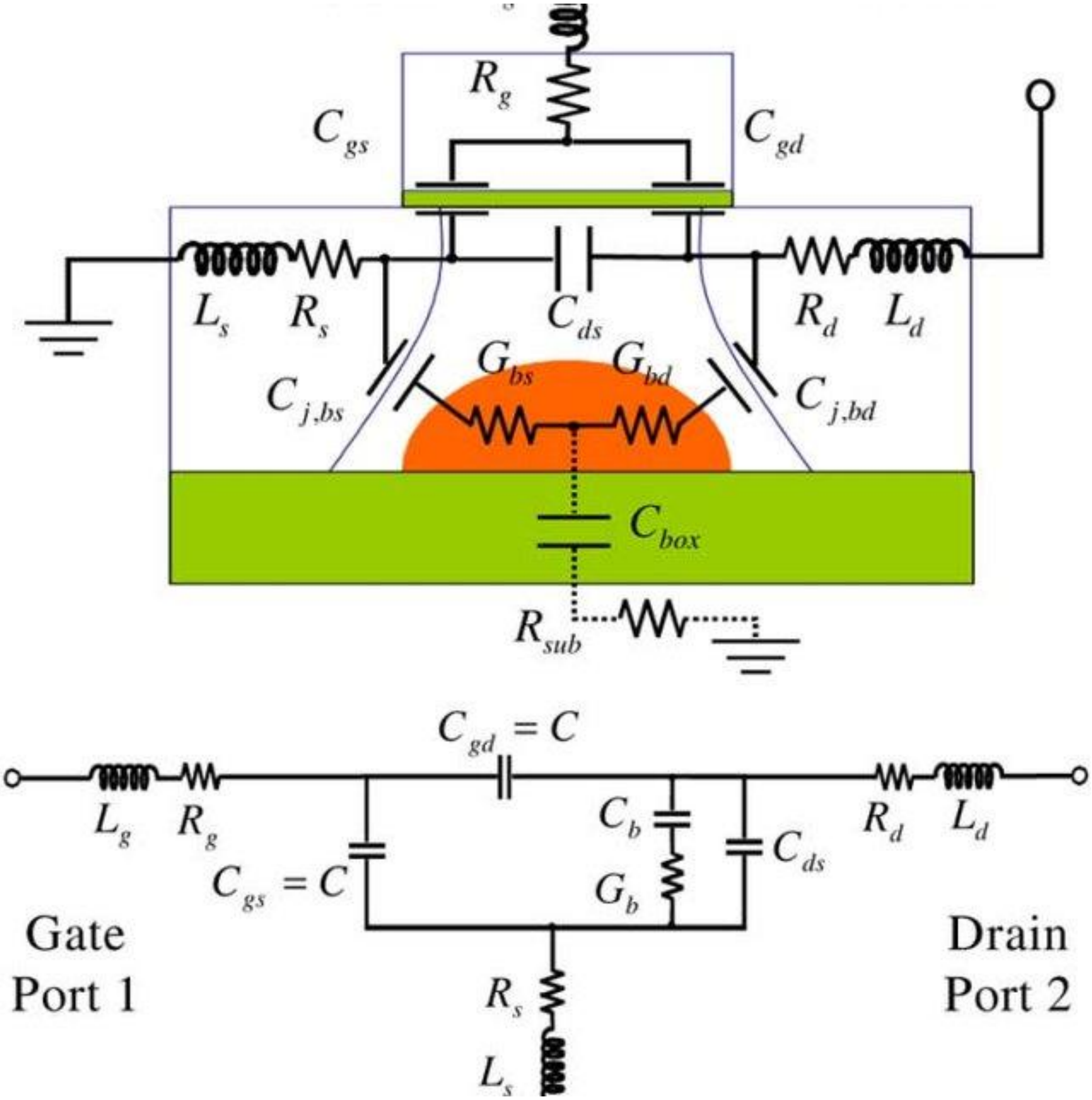

Figure 3.2: Drain Junction Capacitance of SOI MOSFET [26]

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Improved Speed of Stacked Gate

The group of SOI MOSFET is coasting except if the format is outlined intentionally with a view to ground the body. If there should be an occurrence of mass Si MOSFET, where the group of both the draw down transistor is associated with the ground (in instance of NAND gate appeared in figure 3.1), one of the draw down transistor has a negative body predisposition, because of the present streaming to the ground. These outcomes in increment limit voltage and higher fall time, interestingly if this NAND gate is actualized with SOI MOSFETs, the body inclination winds up positive prompting lower limit voltage, bigger deplete current and lower fall time (i.e. enhanced speed).

Small P-N Intersection Leakage Current

The p-n intersection spillage current in SOI structure is little on the grounds that the powerful territory of the p-n intersection other than the side divider zone which is little because of the little thickness of the best silicon layer. This prompts low backup control prerequisite.

Reduced short Channel Effects

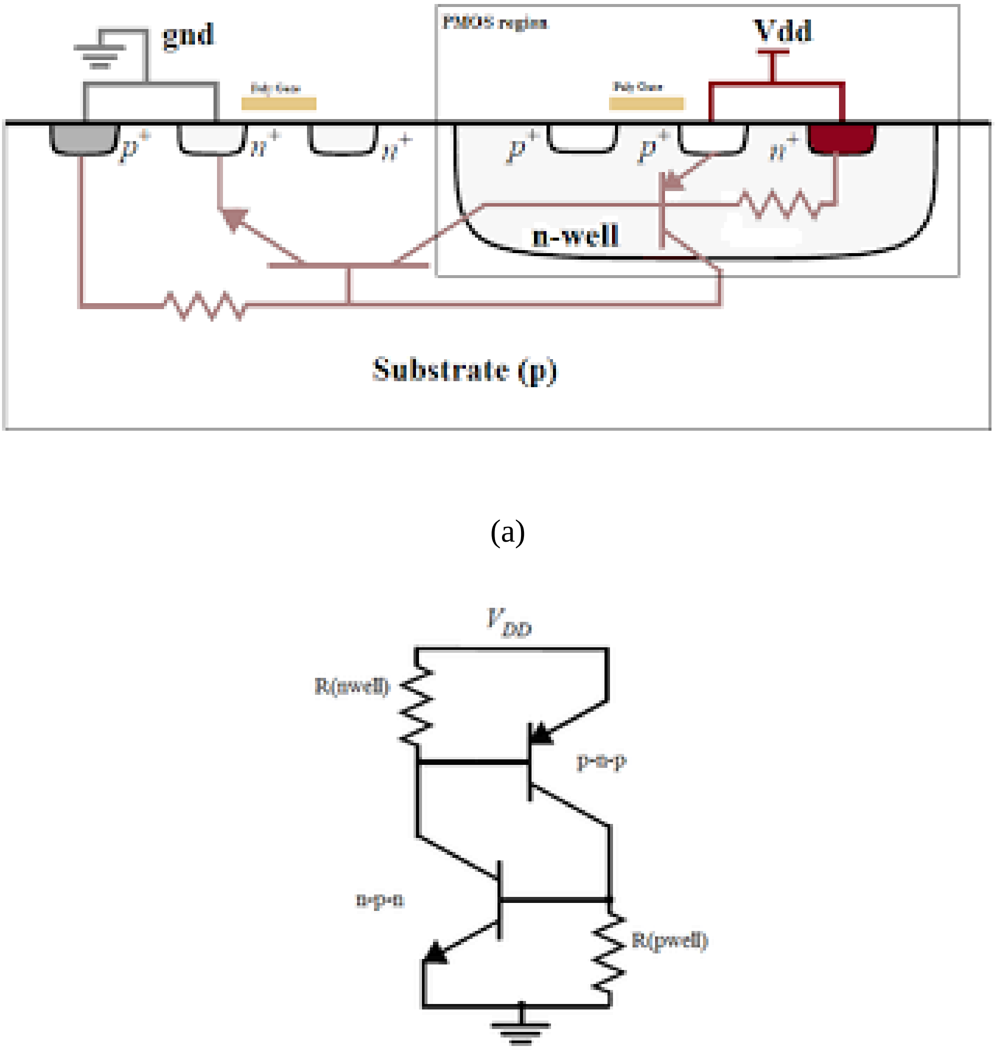
Because the thickness of the body layer and subsequently the profundity of source-deplete intersection in SOI MSOFET is little, so the short channel impacts are extraordinarily diminished notwithstanding for little channel length.

Radiation hardness

Alpha particles produced by follow measure of radio dynamic components ordinarily have vitality of 5 MeV. These particles can enter the Si up to a profundity of 25 µm creating overabundance electron-opening sets in transit. The abundance electron gap sets are adequate to change the memory conditions of a SRAM. In SOI MOSFETs most some portion of the direction of the alpha molecule is underneath the BOX and the electron-opening sets created in the substrate are electrically separated from the dynamic district of the device.

3.3 No Latch Up

Latch-up in CMOS structures executed in mass Si device happens because of parasitic thyristor as appeared in figure 3.3 (a).



(a)

(b)

Figure 3.3: Latch-up in CMOS

This marvel con0strains the greatest working voltages and requires exceptional circuit format to counteract latch up. If there should be an occurrence of SOI CMOS there is no parasitic thyristor (see figure 3.3 b) and accordingly it is free from latch up phenomena.

3.4 Methodology

This chapter focuses on Silvaco Atlas software. It gives an introduction to Silvacosoftware. Then, it follows an explanation of Silvaco atlas parameters. The designing of HfO_2 based Nano-MOSFET is discussed in this chapter.

ATLAS is best utilized with the VWF INTERACTIVE TOOLS. These include DECKBUILD, TONYPLOT, DEVEDIT, MASKVIEWS, and OPTIMIZER. DECKBUILD provides an interactive run time environment.TONYPLOT supplies scientific visualization capabilities. DEVEDIT is an interactive tool for structure and mesh specification and refinement. MASKVIEWS is an IC Layout Editor. The OPTIMIZER supports black box optimization across multiple simulators [i].

3.4.1 SILVACO ATLAS

Silvaco is the short form Silicon Valley Company which is considered as one of the pioneer vendor in technology computer aided design known as TCAD [24]. It was established in 1984. Its head quarter is in Santa Clara, California, USA. The ability to accurately simulate a semiconductor device is somehow critical to industry and research arena. In Silvaco, the Atlas device simulator is specially designed for 2d and 3d modeling with ability to include electrical, optical and thermal properties within a semiconductor device. An integrated platform based on physics, is provided by Atlas to analyze DC, AC and also time domain responses for all semiconductor based technologies [24]. The excellent input syntax always allows the user to design any semiconductor device of any size and design using both user-defined and standard material. There are a good number of examples in ATLAS to give assistance its user. DeckBuild is the run time environment used here in Silvaco ATLAS to input a command file or deck and it has got an extension of ‘‘.in’’.

In order to run the ATLAS in the DeckBuild, one must call the ATLAS simulator first. The command of calling ATLAS simulator is:

go atlas

ATHENA and DevEdit are two other types of simulation software which can be used with Deck Build. Here in our work we have used SILVACO ATLAS only.

3.4.2 Commands Atlas

After calling ATLAS, a syntax structure is to follow so that the ATLAS could execute the command file successfully. Table 3.1 shows the primary group list and statement structure specifications. The basic format of the input file statement is:

<STATEMENT><PARAMETERS>=<VALUE>

Table 3.1: ATLAS command groups with primary statements in each group [24, 32]

Group	Statements
Structure Specification	MESH, REGION, ELECTRODE, DOPING
Material Models specification	MATERIAL, MODEL, CONTACT, INTERFACE
Numerical Method Selection	METHOD
Solution Specification	LOG, SOLVE, LOAD, SAVE
Results Analysis	EXTRACT, TONYPLOT

3.5 Structure specification

Meshing

The Mesh statement is used to define the structure in an inverted 2D or 3D Cartesian grid. The x-axis is positive from left to right; the y-axis is negative from bottom to top. The reason for the inverted y-axis is that the manufacturing coordinates are usually described as depth below the surface. All coordinates are entered in microns and the spacing is used to refine the sharpness and accuracy at an assigned location. ATLAS produces a series of triangles to form the based on the user input parameters. Meshing is done by this command:

One of the meshing is shown in figure 3.4.

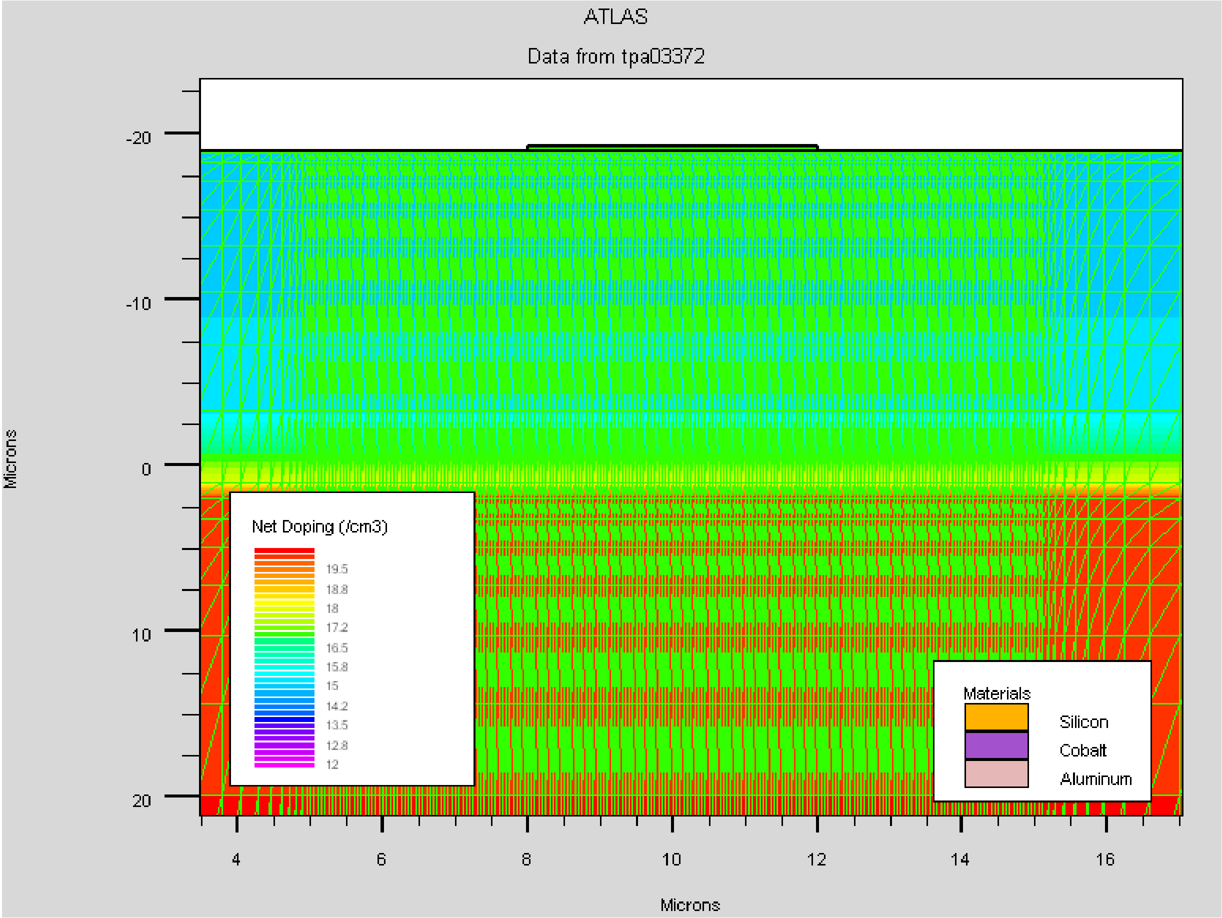


Figure 3.4: Meshing of Semiconductor Device

The first statement:

MESH SPACE.MULT=<VALUE>

This is followed by a series of X.MESH and Y.MESH statements:

X.MESH LOCATION=<VALUE> SPACING=<VALUE>

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>

Regions

The region statement is employed to separate the initial mesh statement into distinct blocks and sets the initial material parameters that may be stated later by number of region. All meshed areas of a structure must be assigned a regions must be order from lowest to highest region. The region command is:

REGION number=<integer><material_type><position parameters>

Electrode

When the regions are set, the electrode should be allotted to the required region so it is often electrically analyzed. The electrodes can be assigned to any region or portion of a region. ATLAS has some fixed names for electrodes e.g. Anode, Cathode, Gate, Source, and Drain.

ELECTRODE <position_parameters>NAME=<electrode name>

The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters.

Doping

The last needed input of the structure specification is that the doping statement. The doping statement is used to allocate the doping level at intervals the previously allocated regions Different properties are often to the doping statement to specify however the semiconductor was doped and of whether the area is n or p type. The following statements were used to define doping parameters:

DOPING <distribution_type><dopant_type><position_parameters=>

The position parameters X.MIN, X.MAX, Y.MIN, and Y.MAX can be utilized rather than a region number.

Material

The material statement relates physical parameters with the materials assigned to the mesh. The important material parameters for most standard semiconductors are already defined by ATLAS and therefore do not require any changes.
For user defined materials, the statement is:
USER.MATERIAL=MATERIAL_NAME

TONYPLOT

TONYPLOT supplies scientific visualization capabilities [i]. The TONYPLOT statement is used to start the graphical post-processor tool. When interpreting the contour plots, it’s important to remember that the solution file contains values only at each node point. The color fills seen in tonyplot are basically interpolations supported the node value. The essential arrangement variables (potential, carrier concentration and so on.) are calculated on the nodes of the nodes of the ATLAS mesh. Along these lines, they are constantly right in TonyPlot.But since ATLAS doesn’t use nodal values of quantities, such as electric field and mobility, the actual values used in calculations cannot be determined from TonyPlot or the structure files. The PROBE statement allows to directly probe values at given locations in the structure. This provides the most accurate way to determine the actual values used in ATLAS calculations.

3.6 Designing of Nano based FDSOI MOSFET

This work is presenting the fabrication of 20 nm FDSOI MOSFET. A fabrication process of 20 nm gate length SOI MOSFET is virtually fabricated through ATLAS module in SILVACO TCAD.

In this experiment firstly define the mesh and then define regions of SiO^2, Silicon as a insulator, and again a layer of SiO^2 is defined. The next procedure is to develop electrode, it should be allotted to the required region so it is often electrically analyzed. Electrodes are namely Gate, Source, Drain, and Substrate. After these step, the doping statement is used allocated the level at intervals the previously allocated regions. P-type surface doping is completed with the concentration of 3×10^{15} atoms per $cm^{-3}$and then n-type completed with 1×10^{20} atoms per cm^{-3}.

The result of the fabrication of SOI MOSFET can be viewed in the TONYPLOT is as shown below. Figure shows the electrodes are highlighted in this structure of this NMOS device. Figure 3.5 shows one of the final structures of designed MOSFET.

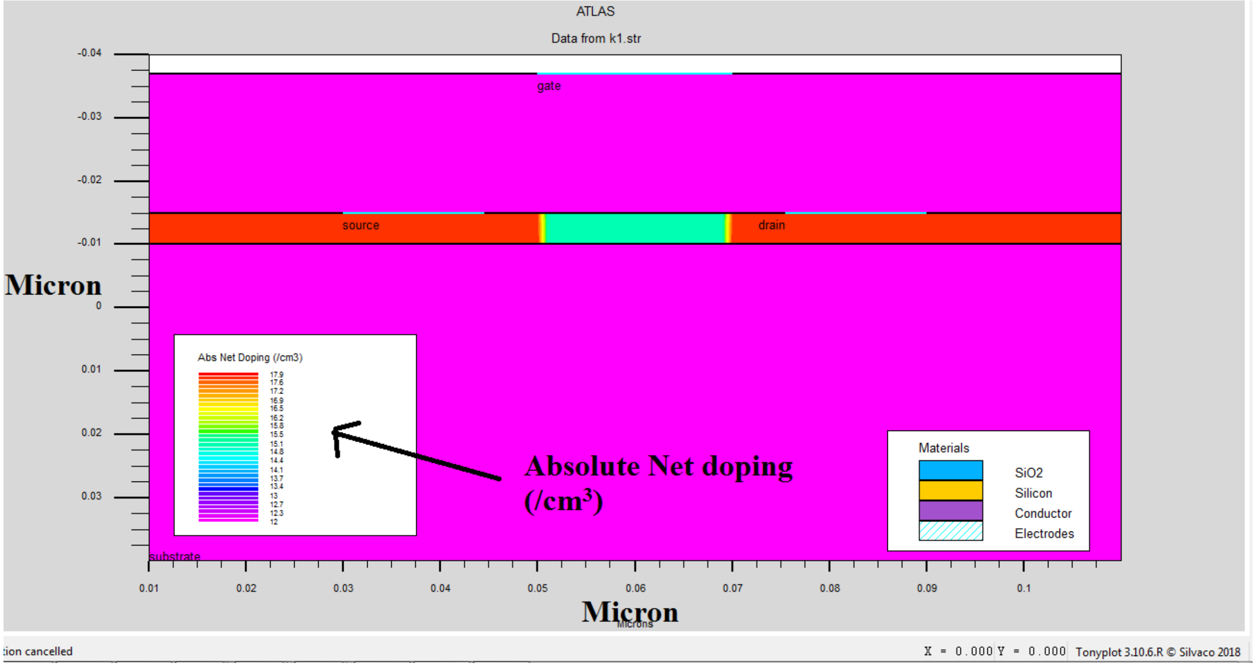


Figure 3.5: Complete structure of 20 nm SOI MOSFET

CHAPTER-4

RESULTS and DISCUSSIONS

In this chapter we discuss about the our designing simulation results.

4.1 Metal Selection

Four different materials have been considered Aluminum, N.poly, W (Tungsten), and WSi_2 (Tungsten Silicide) .I_D-V_{GS} curves have been extracted using ATLAS and graphs are shown below in figure 6.1.It is clear that when Aluminum and N.poly metal are used there is negative threshold voltage are found V_T=-0.560018 V and V_T=-0.394561 V, respectively. So in this this situation we need another material whose gives positive threshold voltage. So we move on the W (Tungsten), and WSi_2 (Tungsten Silicide), and when we using these material we got positive threshold voltage, V_T=0.912903 V and 0.025342 V, respectively.

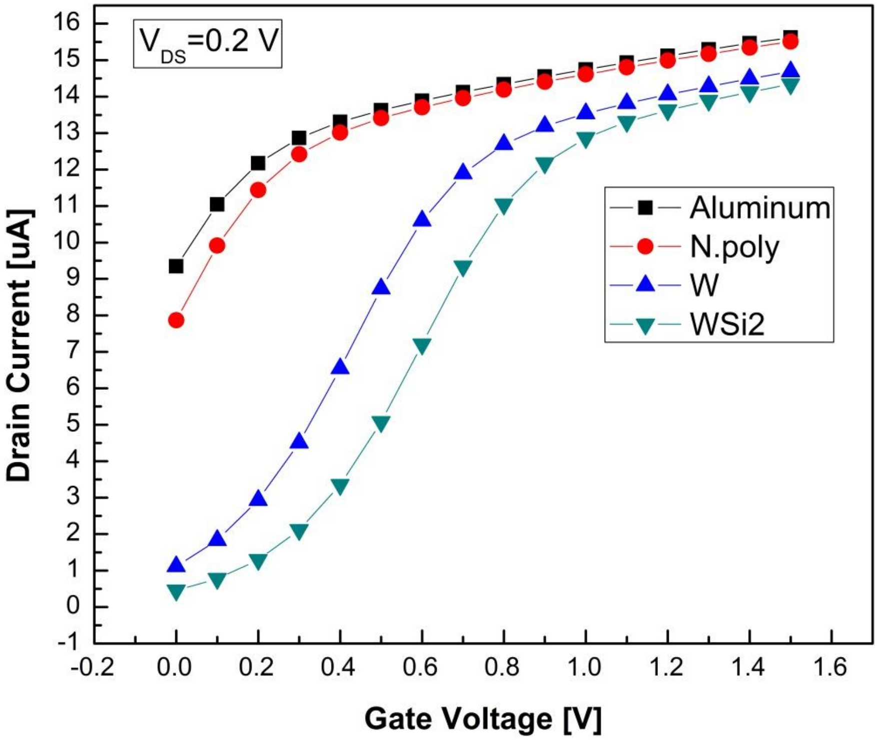


Figure 4.1: I_D-V_{GS} curves for different metal N.poly, Aluminium, W (Tungsten), and WSi_2 (Tungsten Silicide)

Table 4.1: Simulated threshold voltages of different gate metals

Metal	Threshold voltage (V)	Subthreshold Voltage (V/decade)
N. Poly	-0.394561	0.996183
Aluminum	-0.560018	1.37839
W (Tungsten)	0.0912903	0.462334
WSi_2 (Tungsten Silicide)	0.253420	0.435528

4.2 I_D versus V_{GS} Characteristics

Figure 4.2 shows the variation of drain current at different drain to source voltage. From figure it can be observed that as drain to source voltage is increasing drain current is also increasing respectively.

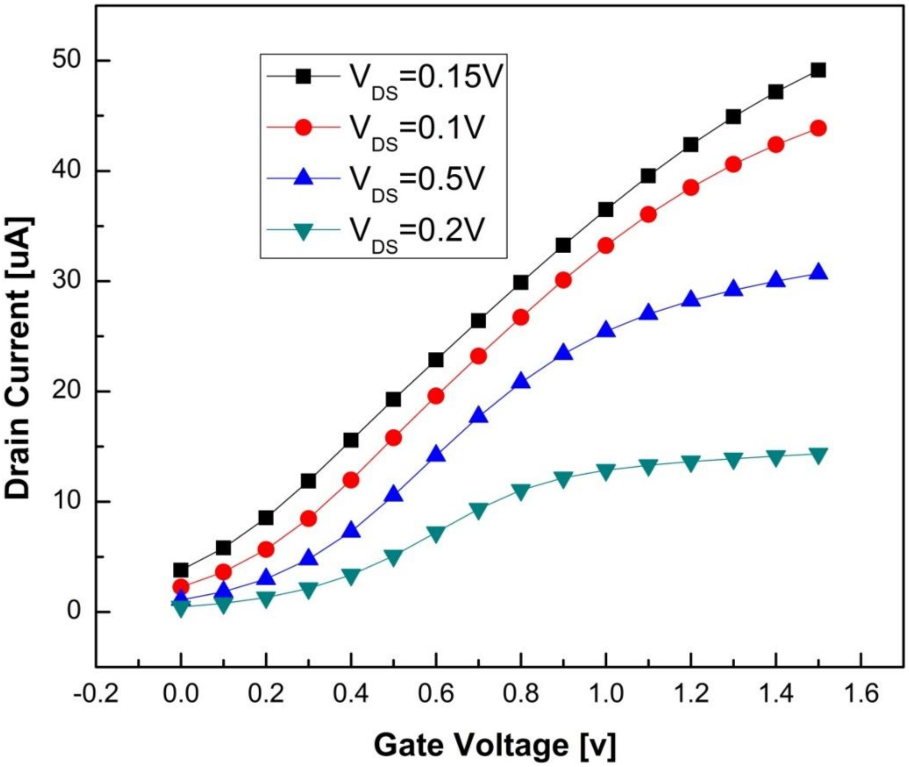


Figure 4.2: I_D vs. V_{GS} curves

4.3 Variation of I_D as Function of V_{DS}

Figure indicates the families of I_D vs V_{DS} curves for SOI MOSFET. Plot of drain current with respect gate voltage V_{GS}=0.7 V, 0.1 V, and 1.5 V of SOI MOSFET and V_D varying from 0 V to 1.5 V. As expected it has been observed that the drain current increases with the increase of drain to source voltage.

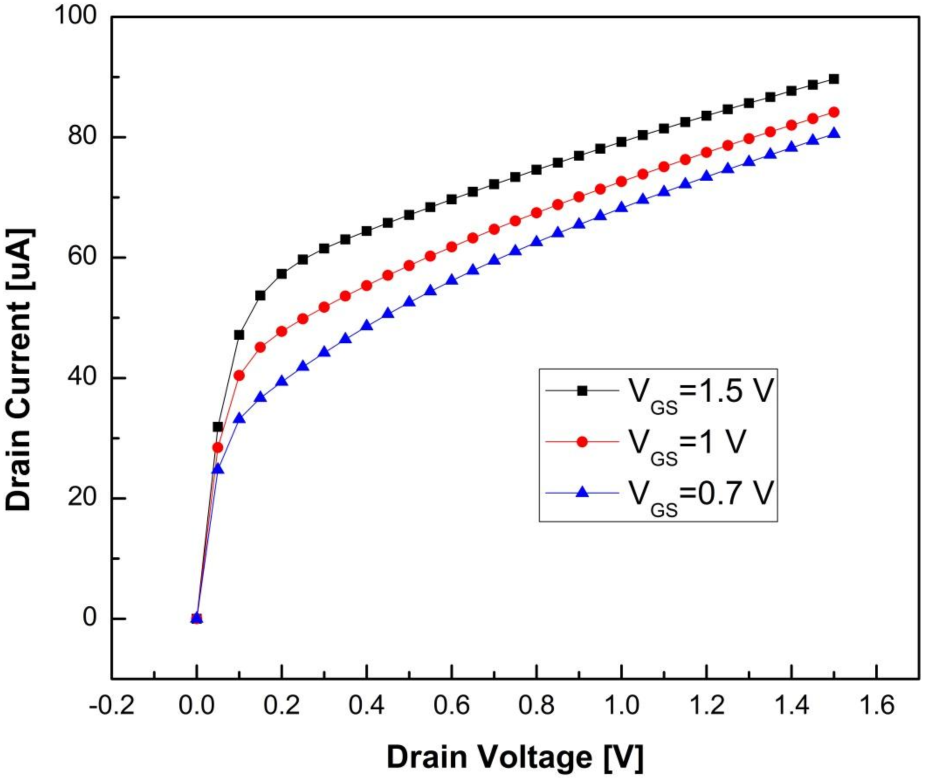


Figure 4.3: I_D vs V_{DS} curve

CHAPTER-5

CONCLUSION and FUTURE SCOPE

5.1 Conclusion

The bulk Si MOSFET has been the principle gadget shaping the foundation of the improvement of ultra-high thickness ICs. Be that as it may, because of ceaseless scaling down, a circumstance has achieved, where the execution parameters of the MOSFETs are corrupted (due to the fundamental physical cutoff points), to the degree that it is exceptionally hard to create ICs with nano-scale mass MOSFETs. Another age gadget, which can offer great execution parameters i.e. low power utilization and fast, notwithstanding for nano-sacle gadgets, is required.

5.2 Future scope

The SOI is a marvelous discovery in the field of microelectronics and a breakthrough technology with a robust future. It’s an innovation that will allow the semiconductor industry continue to deliver an ever better experience for consumers on next generation digital devices.SOI will enable the device to operate faster. It is a simpler way to deliver these benefits compared to other alternatives and is available for design and manufacturing today

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Performance Evaluation of Fully Depleted Silicon on Insulator MOSFET

Yogendra Kumar Sharma
Department of ECE
Integral University
Lucknow, India
yogendras@student.iul.ac.in

Imran Ullah Khan
Department of ECE
Integral University
Lucknow, India
iukhan@iul.ac.in

Performance Evaluation of Fully Depleted Silicon on Insulator MOSFET

***Abstract*— VLSI technology development nowadays is mostly focused on the downsizing of semiconductor devices, which is significantly reliant on advancements in complementary metal oxide semiconductor technology. Due to capacitance, shorter channel length, body biassing, faster switching transistor, limited variability, and faster running transistor, Silicon-on-Insulator technology has seen a lot of changes. In comparison to traditional bulk technology, Silicon on Insulator offers intriguing new possibilities. The recent stalling of advancement in CMOS technology has been noticed. Fully depleted silicon on insulator provides additional performance. Power usage and communication speed are two areas where performance can be improved. Silicon on insulator technology has the potential to reduce power consumption by nearly half while increasing speed by about 40%. Using the Atlas module of the SILVACO software, the research presents a comprehensive analysis of silicon on insulator based nano metal oxide semiconductor field effect transistors. Atlas is used to virtually construct a 20 nm silicon on insulator MOSFET. The gate metals employed are Aluminum, N. poly, W (Tungsten), and WSi2 (Tungsten Silicide), and their respective characteristics are obtained and compared. Finally, WSi2 was chosen as the final gate metal because it has the desired band offset, resulting in a positive threshold voltage without the need for any further implants in the channel region. Other metrics are collected, such as the variation of ID vs. VGS features at various values. There is also a fluctuation in drain current as a function of drain to source voltage.**

Keywords- MOSFET, Fully depleted, Silicon on Insulator, SILVACO, Tungsten Silicide.

I. INTRODUCTION

For several years, the semiconductor industry has seen an exponential increase in the number of transistors per integrated circuit. Moore's law predicted that this would happen. The advancement of silicon-based CMOS technology has aided the evolution of electronics, information technology (IT), and communication. The scaling of its dimensions allows for ongoing progress. CMOS scaling is the main driving factor of Silicon technology innovation, as it improves both device density and performance.

A semiconductor layer, such as germanium, is structured over a

protector layer, which might be a covered oxide layer framed on a semiconductor substrate in a Silicon on Insulator (SoI) Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

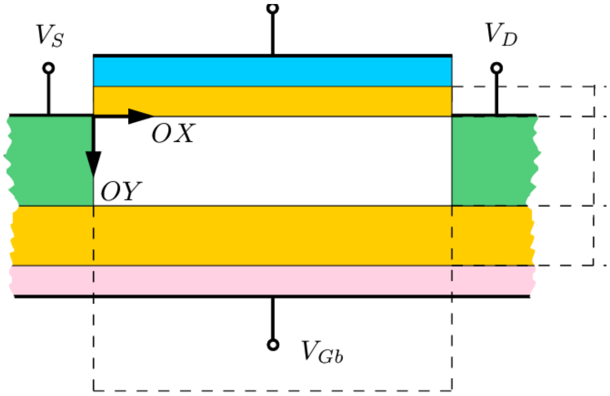


Figure 1. Idealized geometry of the SoI MOSFET [1]

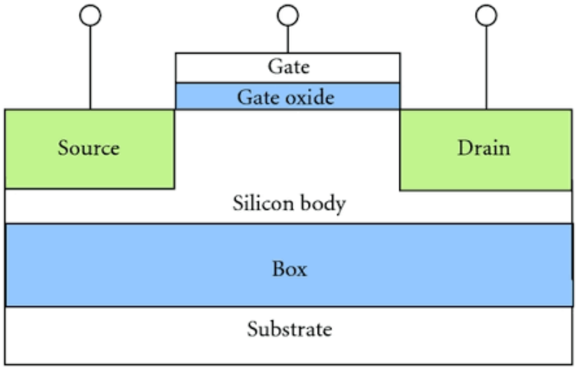


Figure 2. SoI MOSFET structure [1]

There are two kinds of silicon on encasing MOSFET

1. Partially Depleted (PD) SoI MOSFET
2. Fully Depleted (FD) SoI MOSFET

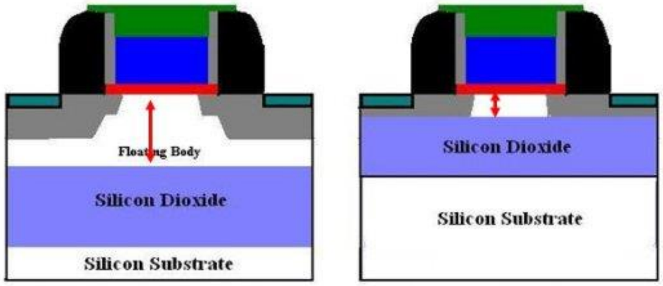


Figure 3. Partially Depleted and Fully depleted SOIMOSFET [2]

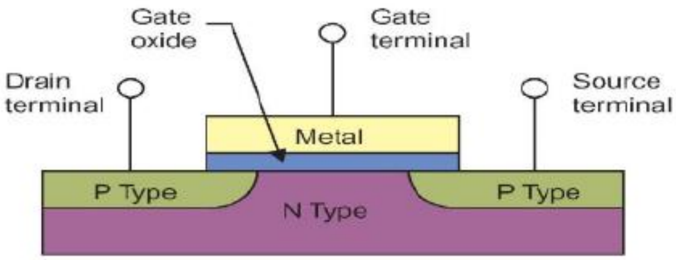


Figure 4. Cross sectional of MOSFET [2]

The fundamental device conditions of PD SOI MOSFETs are the same concerning mass devices [1-5], with the exception of obviously from the intricacies emerging from the drifting body (FBE).

II. Fully Depleted SOI MOSFETs

In FDSOI case, the front and back channels are electro-statically coupled during device operation. This electrostatic coupling makes the front channel FD SOI parameters subject to the back gate Voltage, including channel current, edge voltage, sub-limit incline and so on.

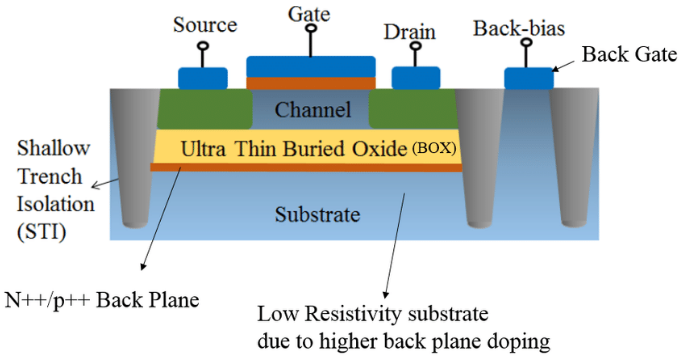
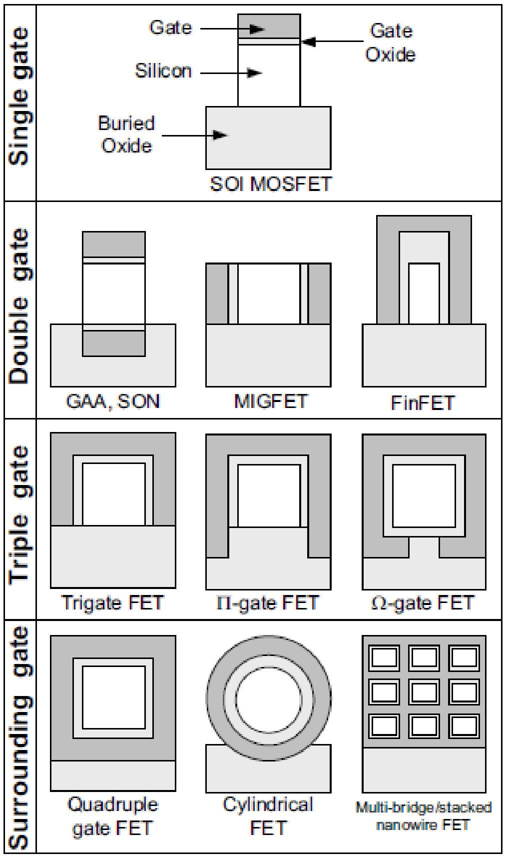


Figure 5. Fully depleted SOI MOSFET [3]

A. MOSFET Scaling

MOSFET miniaturisation is highly desirable for a variety of reasons. The first and most fundamental reason for shrinking transistor sizes is to fit an increasing number of devices into a given chip area. As a result, the chip has more functionality in the same space. The number of chips that may be generated per wafer determines the cost per integrated circuit. As a result, shrinking the size of ICs allows for more chips per wafer, lowering the price per chip. Over the last 30 years, the number of transistors per chip has been doubled every 23 years once a new technology is launched. The number of MOSFETs in a microprocessor, for example, produced in a 45nm technology will be twice [7-9]



].

Figure 6. Different Gate Structures in reference to FDSOI

B. Moore's Law

In the year 1965, Gordon Moore made a tremendous and vital observation according to which in every 18 or 24 months or so the number of devices on a chip gets doubled. Moore's law shows a continuous miniaturization. A new technology node is introduced or a new technology generation is introduced with the reduction of minimum line width. Some of the examples of the technology generation or technology node is shown in table 1.

Table 1. Improvement in technology Node over the years

Year	2004	2006	2008	2010	2011	2013	2016	2022
Technology Node	90 nm	65 nm	45 nm	32 nm	22 nm	16 nm	14 nm	10 nm

III. NEED OF SILICON ON INSULATOR

To improve the user experience and produce better digital devices, transistor sizes must be reduced while performance and power consumption are increased. The gate length decreases as the transistor shrinks. The transistor's control over the channel region is likewise diminished, decreasing its performance. Even when the transistor is turned off, some undesirable leakage current occurs [8, 9]. To reduce leakage current while still delivering a high-performance bulk Silicon transistor, manufacturers have become increasingly complicated, adding new levels of manufacturing complexity at an increasing rate. In terms of technology, a new 20nm solution is required to minimise complexity while delivering the industry-expected benefits of reduced silicon geometry.

A. Shorter Channel Length

The SOI transistor has the shorter effective channel as compared to bulk Si Simplification. The shorter channel reduces the the time necessary for the electron flow from source to drain leading to a faster transistor. In order to improve the transistor performance a voltage can be applied to the substrate this method is body biasing facilitates the creation of the channel between the source and drain which result in faster switching transistor.

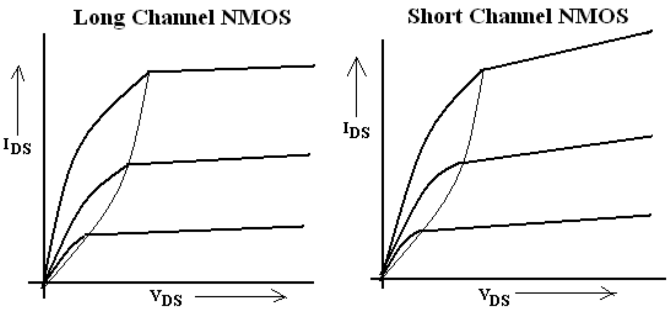


Figure 7. Effect of Channel Length Modulation [5]

A. B.Body Biasing and Faster Switching Transistor

The biasing creates a buried gate below the channel making the SOI act like a vertical double gate transistor. In bulk technology the ability to do body biasing is very limited due to parasitic current leakage. The buried gate in the SOI transistor prevents any leakage in the substrate. This allows a much higher voltage on the body leading to a significant boost in the performance. In a chip there are billions of transistors characteristics of each transistor are not exactly because the different quantities of dopants injected into the channel during the manufacturing process is the same [10-15].

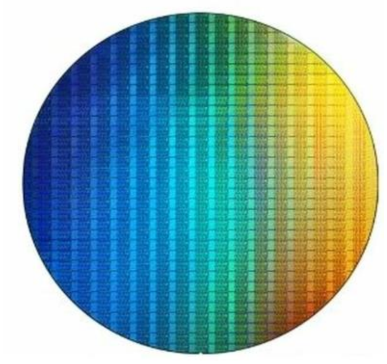


Figure 8. SOI Wafer [6]

In SOI, dopants usage is greatly reduced thereby limiting the variability results characteristics of each transistor is closely to average in the process. This allows transistor runs faster for a given voltage. SOI chip is able to operate at lower voltage than delivers the same performance. SOI attractive with lower power consumption.

IV. METHODOLOGY

This chapter focuses on Silvaco Atlas software. It gives an introduction to Silvacosoftware. Then, it follows an explanation of Silvaco atlas parameters. The designing of HfO_2 based Nano-MOSFET is discussed in this paper [16-20].

ATLAS is best utilized with the VWF INTERACTIVE TOOLS. These include DECKBUILD, TONYPLOT, DEVEDIT, MASKVIEWS, and OPTIMIZER. DECKBUILD provides an interactive run time environment.TONYPLOT supplies scientific visualization capabilities. DEVEDIT is an interactive tool for structure and mesh specification and refinement. MASKVIEWS is an IC Layout Editor. The OPTIMIZER supports black box optimization across multiple simulators [20].

B. A. SILVACO ATLAS

C.

Silvaco is the short form Silicon Valley Company which is considered as one of the pioneer vendor in technology computer aided design known as TCAD [24]. It was established in 1984. Its head quarter is in Santa Clara, California, USA. The ability to accurately simulate a semiconductor device is somehow critical to industry and research arena. In Silvaco, the Atlas device simulator is specially designed for 2d and 3d modeling with ability to include electrical, optical and thermal properties within a semiconductor device. An integrated platform based on physics, is provided by Atlas to analyze DC, AC and also time domain responses for all semiconductor based technologies [21-25]. The excellent input syntax always allows the user to design any semiconductor device of any size and design using both user-defined and standard material. There are a good number of examples in ATLAS to give assistance its user. DeckBuild is the run time environment used here in Silvaco ATLAS to input a command file or deck and it has got an extension of ‘‘.in’’.

In order to run the ATLAS in the DeckBuild, one must call the ATLAS simulator first. The command of calling ATLAS simulator is:

go atlas

ATHENA and DevEdit are two other types of simulation software which can be used with Deck Build. Here in our work we have used SILVACO ATLAS only.

B. Commands Atlas

After calling ATLAS, a syntax structure is to follow so that the ATLAS could execute the command file successfully. Table 3 shows the primary group list and statement structure specifications. The basic format of the input file statement is:

```
<STATEMENT><PARAMETERS>=<VALUE>
```

C. Structure specification

The Mesh statement is used to define the structure in an inverted 2D or 3D Cartesian grid. The x-axis is positive from left to right; the y-axis is negative from bottom to top. The reason for the inverted y-axis is that the manufacturing coordinates are usually described as depth below the surface. All coordinates are entered in microns and the spacing is used to refine the sharpness and accuracy at an assigned location. ATLAS produces a series of triangles to form the based on the user input parameters. Meshing is done by this command:

One of the meshing is shown in figure 8.

The first statement:

```
MESH SPACE.MULT=<VALUE>
```

This is followed by a series of X.MESH and Y.MESH statements:

```
X.MESH LOCATION=<VALUE> SPACING=<VALUE>
```

Table 2. ATLAS command groups with primary statements in each group [24, 25]

Group	**Statements**
Structure Specification	MESH, REGION, ELECTRODE, DOPING
Material Models specification	MATERIAL, MODEL, CONTACT, INTERFACE
Numerical Method Selection	METHOD
Solution Specification	LOG, SOLVE, LOAD, SAVE
Results Analysis	EXTRACT, TONYPLOT

```
Y.MESH LOCATION=<VALUE> SPACING=<VALUE>
```

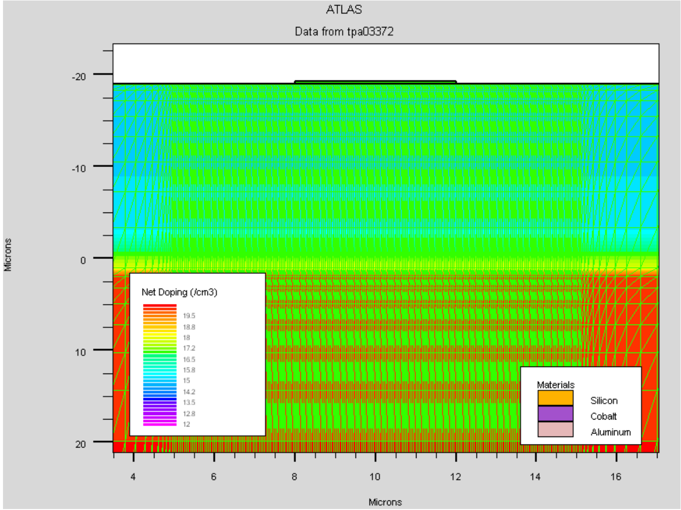


Figure 9. Meshing of Semiconductor Device

D.

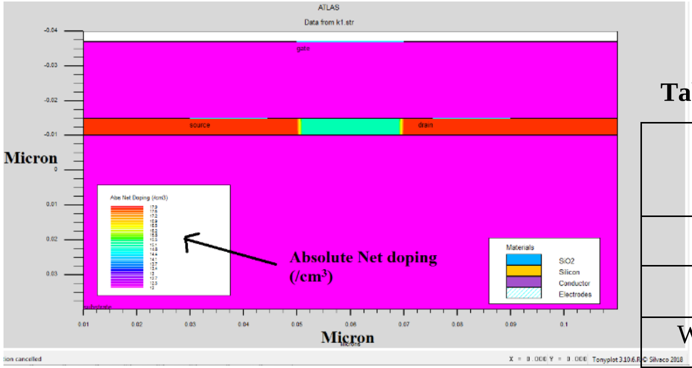


Figure 10. Complete structure of 20 nm SOI MOSFET

V. METAL SELECTION

Four different materials have been considered Aluminum, N.poly, W (Tungsten), and WSi$_2$ (Tungsten Silicide) .I$_D$-V$_{GS}$ curves have been extracted using ATLAS and graphs are shown below in figure 6.1.It is clear that when Aluminum and N.poly metal are used there is negative threshold voltage are found V_T=-0.560018 V and V_T=-0.394561 V, respectively. So in this this situation we need another material whose gives positive threshold voltage. So we move on the W (Tungsten), and WSi$_2$ (Tungsten Silicide), and when we using these material we got positive threshold voltage, V_T=0.912903 V and 0.025342 V, respectively.

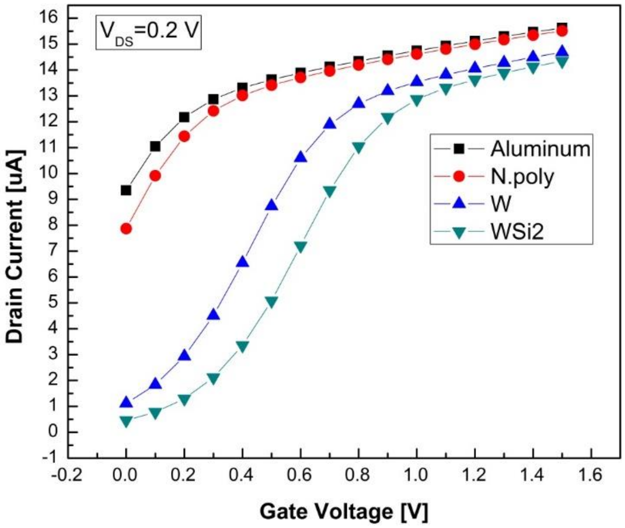


Figure 11. I$_D$-V$_{GS}$ curves for different metal N.poly, Aluminium, W (Tungsten), and WSi$_2$ (Tungsten Silicide)

Table 3. Simulated threshold voltages of different gate metals

Metal	Threshold voltage (V)	Subthreshold Voltage (V/decade)
N. Poly	-0.394561	0.996183
Aluminum	-0.560018	1.37839
W (Tungsten)	0.0912903	0.462334
WSi$_2$ (Tungsten Silicide)	0.253420	0.435528

A. I$_D$ versus V$_{GS}$ Characteristics

Figure 10 shows the variation of drain current at different drain to source voltage. From figure it can be observed that as drain to source voltage is increasing drain current is also increasing respectively.

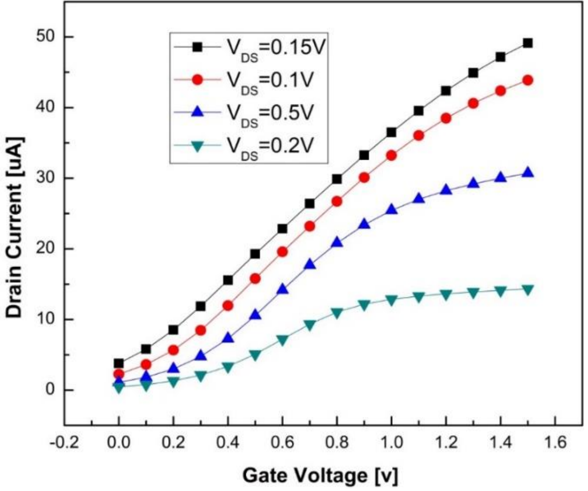


Figure 12. I$_D$ vs. V$_{GS}$ curves

B. Variation of I$_D$ as Function of V$_{DS}$

Figure indicates the families of I$_D$ vs V$_{DS}$ curves for SOI MOSFET. Plot of drain current with respect gate voltage V$_{GS}$=0.7 V, 0.1 V, and 1.5 V of SOI MOSFET and V$_D$ varying from 0 V to 1.5 V. As expected it has been observed that the drain current increases with the increase of drain to source voltage.

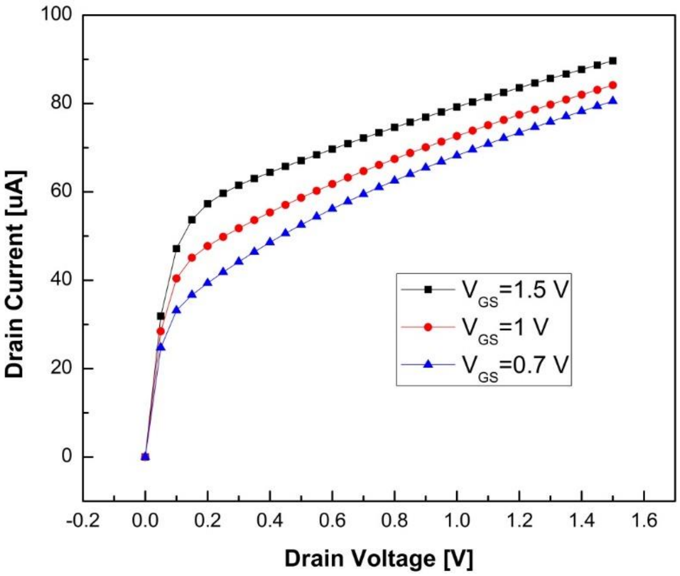


Figure 13. I_D vs V_{DS} curve

VI. CONCLUSION

The bulk Si MOSFET has been the principle gadget shaping the foundation of the improvement of ultra-high thickness ICs. Be that as it may, because of ceaseless scaling down, a circumstance has achieved, where the execution parameters of the MOSFETs are corrupted (due to the fundamental physical cutoff points), to the degree that it is exceptionally hard to create ICs with nano-scale mass MOSFETs. Another age gadget, which can offer great execution parameters i.e. low power utilization and fast, notwithstanding for nano-sacle gadgets, is required.

VII. FUTURE SCOPE

The SOI is a marvelous discovery in the field of microelectronics and a breakthrough technology with a robust future. It's an innovation that will allow the semiconductor industry continue to deliver an ever better experience for consumers on next generation digital devices.SOI will enable the device to operate faster. It is a simpler way to deliver these benefits compared to other alternatives and is available for design and manufacturing today.

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