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Simulation of Carbon Nanotube FETs for Power-Efficient Digital Circuits

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Abstract— This work addresses the limitations of silicon scaling by exploring Carbon Nanotube FETs (CNTFETs) as alternatives. Schottky Barrier CNTFETs (SBCNTFETs) suffer from ambipolar currents, which reduce the I_{ON}/I_{OFF} ratio; this can be improved through optimised design parameters. A Double Gate (DG) structure is modelled to enhance gate control, achieving better I_{ON}/I_{OFF} ratio (5.55×10^5) and subthreshold swing (87.3 mV/decade). A mathematical model for DG-SBCNTFET is developed and validated with Nano TCAD ViDES simulations. Using optimised parameters, a DG-SBCNTFET-based 6T SRAM cell is designed and simulated in HSPICE, demonstrating 20% lower power dissipation compared to a conventional CNTFET SRAM cell without compromising stability.

Keywords- ***CNTFET, 6T-SRAM cell, SBCNTFET, CMOSFET***

I. INTRODUCTION

Carbon nanotubes (CNTs) are nanostructures created by rolling a single graphene sheet into seamless, hollow cylinders. Although thousands of times thinner than a human hair, they can grow to several micrometres in length, resembling a hair strand in form but not in scale of thickness. Based on their structure, CNTs are generally classified as single-walled (SWCNTs) or multi-walled (MWCNTs), each exhibiting distinct physical and electronic properties [1]. As shown in Figure 1, this classification depends on whether one or multiple graphene layers are rolled into a tube. Studies have demonstrated that chemically doping CNTs to n-type significantly improves CNTFET performance [2]. Furthermore, controlled doping allows conversion of p-type CNT devices into n-type, resulting in higher on-currents in the devices [3,4]. When bandgap is absent, the nanotube behaves like a metal. In table 1 basic comparison between silicon and single wall carbon nano tube is shown. It covers basic properties like electron mobility, bandgap, diameter and electron phonon mean free path, from the table it is clear that carbon nano tube single walled structure is advance version of silicon.

TABLE I: COMPARAISION BETWEEN SILICON AND CNTSW
RANGE OF DIELECTRIC CONSTANT

Parameter	Silicon	CNTSW
Electron Mobility (cm^2/V-sec)	1400	20000
Bandgap (eV)	1.12	0.9
Diameter (nm)	~ 6	0.6 ~1.8
Electron Phonon Mean free path (Å)	76	~ 700

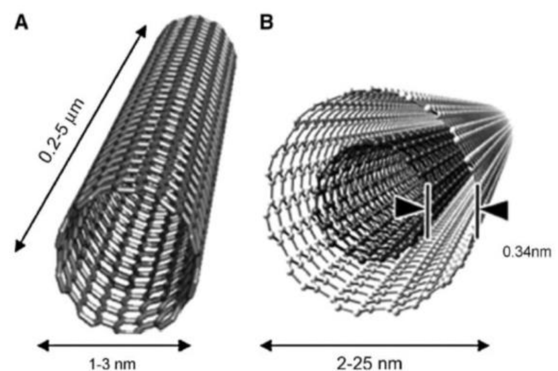

Fig.1. Structure of single wall and multi-wall CNTs [7]

Figure 1 shows structure of single wall CNT and multiwall CNT (CNTSW and CNTMW) [7]. Figure 2 shows applications and properties of CNT, it includes electrical, mechanical, thermal and optical properties and there corresponding applications. Figure 3(a) and (b) shows the schematic of a carbon Nanotube field effect transistor [9, 10], respectively.

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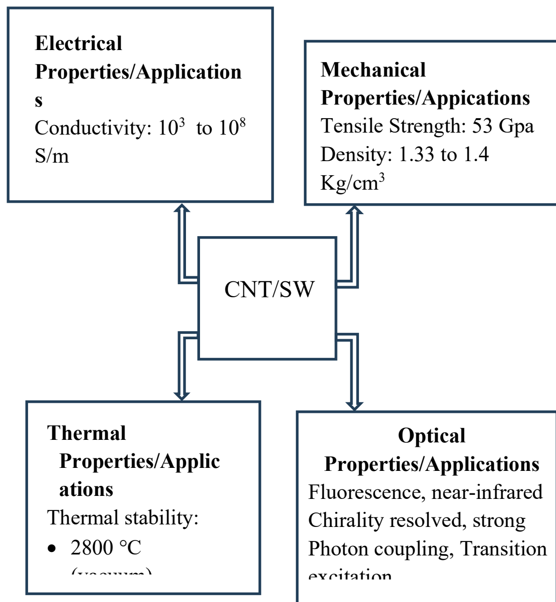

Fig.2. Properties & applications of CNT

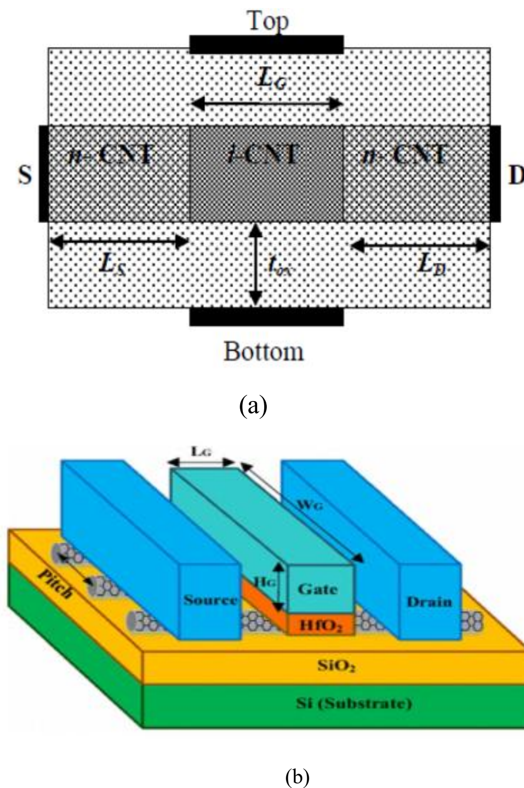

Fig 3. (a) & (b) Schematic of carbon Nanotube field effect transistor [9]

II. COMPARISON OF CNTFETS AND MOSFETS

- When CNT is compared with traditional MOSFETs higher carrier mobility can be achieved by applying high K (dielectric constant). CNTFET have higher carrier mobility [11].
- The channel length in CNTFET is less than 10 nm, as compared to taraditional MOSFET in which it is around 14nm to get the better carrier transport in CNTFET.
- Chirality is lower in CNTFT as compared to traditional MOS leads to faster switching along and lower power dissipation [12, 13].
- By modulating the contact resistance switching capacity of CNTFET can be increased.
- In CNTFET there is better control of gate which results in higher transconductance as much as four times in CNTFET.

III. METHODOLOGY

Methodology of the proposed work includes the above blocks from architecture identification to further process. Figure 4 shows the methodology, it includes selection, development, analysis, low power design and finally benchmark development for proposed design.

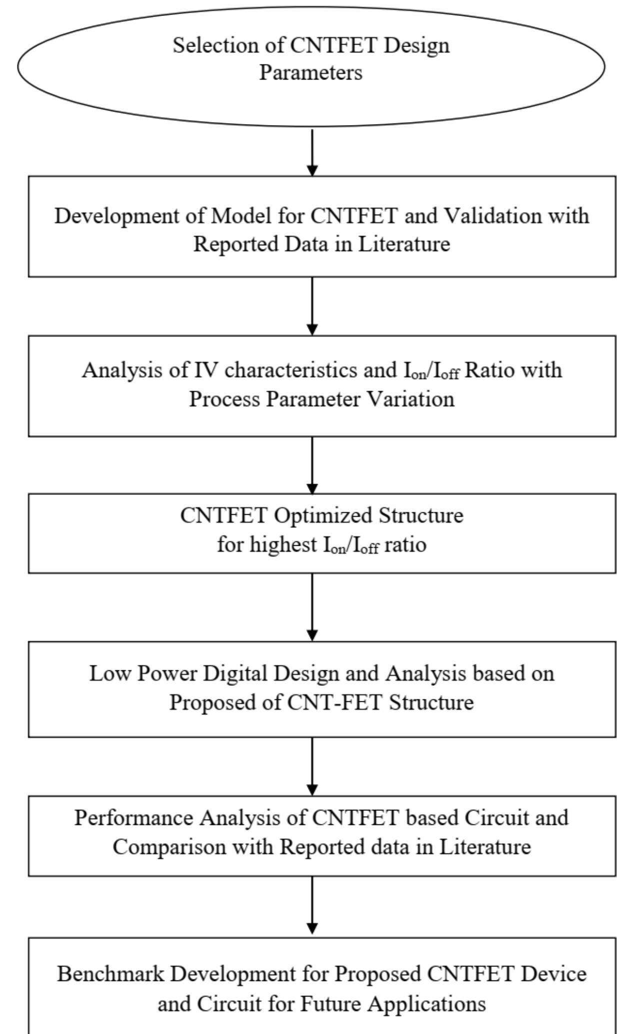

Fig. 4. Methodology of proposed work

IV. SIMULATION RESULT AND ANALYSIS

In the paper design and simulation of proposed DG-SBCNTFET based 6T-SRAM cell by using optimized parameters carried out. A Comparison of DG-SBCNTFET

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based 6TSRAM cell to that of the conventional CNTFET based SRAM cell is presented on the basis of stability and power dissipation [14, 15].

TABLE II: CHIRALITY EFFECT ON I_{ON}/I_{OFF} RATIO AND SUBTHRESHOLD SLOPE

S.No.	Chirality (x,0)	I_{ON}/I_{OFF} Ratio	Subthreshold Slope
1.	10	902000	97.4
2.	13	2000	112
3.	16	341	137
4.	19	66.5	161
5.	22	15.3	214
6.	25	4.0	367

TABLE III: I_{ON}, I_{OFF} RATIO VS OXIDE THICKNESS FOR VARYING DIELECTRIC CONSTANT

S. No.	Oxide Thickness	I_{ON}/I_{OFF} ratio				
		k=3.9	k=11	k=16	k=25	k=30
1	0.15	195	230	235	243	245
2	0.25	180	210	230	240	243
3	0.5	160	208	225	235	240
4	1	145	195	220	230	235
5	1.5	140	190	216	226	231
6	2	136	186	210	220	228
7	2.5	125	180	205	215	225
8	3	120	175	200	210	220
9	3.5	115	170	195	205	210
10	4	110	165	190	200	205

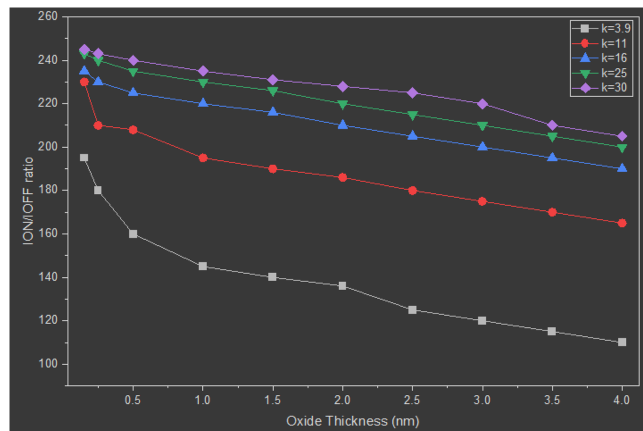

Fig. 5. Comparative analysis: I_{ON}/I_{OFF} ratio and oxide thickness with varying dielectric constant (k)

The table II and III presents the variation of the I_{ON}/I_{OFF} ratio and oxide thickness with varying dielectric constant (k). It is observed that for very thin oxide layers (0.15–0.5 nm), the ratio remains relatively high across all k values, reaching a maximum of 245 for 0.15 nm at (k=30). The ratio decreases steadily with oxide thickness from 1 nm-4 nm, the ratio, indicating a degradation in device performance due to increased leakage suppression and reduced drive current. Additionally, for a given oxide thickness, higher dielectric constant values improve the ratio, though the improvement is more pronounced for thinner oxides. This demonstrates the effectiveness of high-k materials in maintaining performance while allowing thicker physical oxides, thereby reducing gate leakage. Overall, the data highlights that ultra-thin oxides combined with high-k dielectrics provide the best trade-off for achieving maximum ratios. Figure 6 and 7 shows design flow and 6T SRAM cell carbon nano tube FET structure.

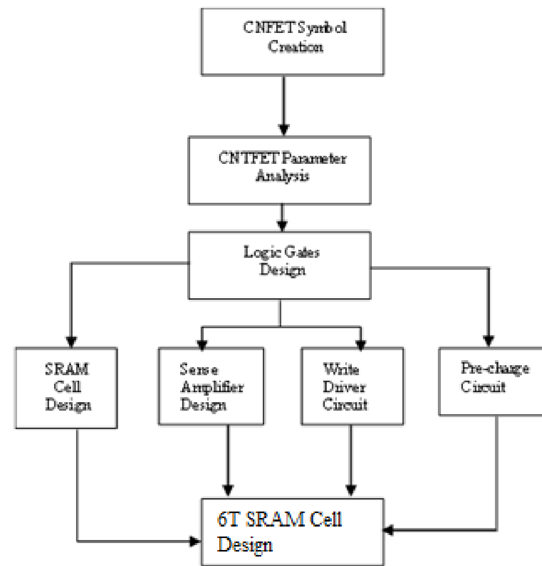

Fig.6. Design Flow 6T SRAM cell using CNTFET

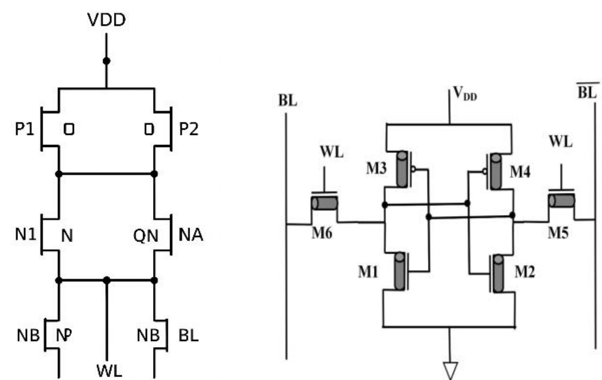

Fig.7. 6T SRAM cell using CNTFET structure

Figure 8 shows basic curves of carbon nano tube field effect transistor write/read modes and internal node voltages. Table IV shows comparative analysis of basic CNTFET and DGSBCNTFET for a value of V_{DD} as 0.9 Volt.

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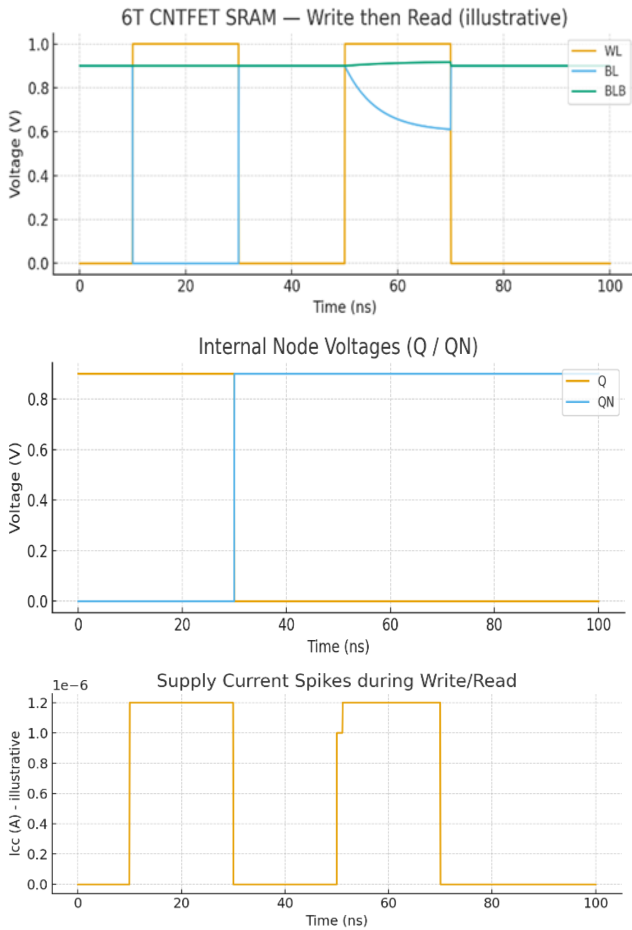

Fig.8. 6T CNTFET SRAM Graphs

TABLE IV: COMPARISON OF VARIOUS PERFORMANCE PARAMETERS OF SRAM FOR CONVENTIONAL CMOS CNTFET AND DG-SBCNTFET AT VDD=0.9V

S.No.	Parameters/Device	Conventional CMOS CNTFET [15, 16]	DG-SBCNTFET
1.	Static Power (pW)	27	22
2.	Static- Noise-Margin (SNM)(mV)	250	260
3.	Read SNM (mV)	166	158
4.	Write SNM (mV)	405	420

Equations involves in the design are as follows:

$$D_{CNT}=\frac{a\sqrt{m^2+mn+n^2}}{\pi} \qquad (1)$$

- a Lattice constant (0.246 nm),
- m and n - chirality indices

The gate oxide thickness determines the gate capacitance [13].

$$t_{ox} = \frac{K_{ox} \cdot \varepsilon_o}{C_{ox}} \qquad (2)$$

Where C_{ox} is Gate oxide capacitance per unit area

ε_0 is permittivity of free space

K_{ox} is dielectric constant of the gate oxide and t_{ox} is thickness of the gate oxide [14].

Gate oxide dielectric constant K_{ox} relates to the gate oxide material and affects C_{ox} [15].

$$K_{ox} = \frac{C_{ox} \cdot t_{ox}}{\varepsilon_o} \qquad (3)$$

The substrate dielectric constant K_{sub} impacts the capacitive coupling between the channel and the substrate.

$$K_{sub} = \frac{C_{sub} \cdot t_{sub}}{\varepsilon_o} \qquad (4)$$

Where t_{sub} is Thickness of the substrate layer and $Csub$ is Substrate capacitance.

The spacer dielectric constant K_{spa} determines the fringe capacitance in the device.

$$K_{spa} = \frac{C_{spa} \cdot t_{spa}}{\varepsilon_o} \qquad (5)$$

Where t_{spa} is Thickness of the spacer dielectric layer [21].

The energy difference E_V at the source and drain, influencing carrier injection

$$E_V = E_{fs} - E_g \qquad (6)$$

Where E_{fs} is Fermi level and E_g is Bandgap energy [14].

Doping density E_{fsd} influences the shift in the Fermi level.

$$E_{fsd} = q.N_d.t_{ch} \qquad (7)$$

Where N_d is Doping concentration and t_{ch} is Channel thickness [15].

DG SB CNTFETs used in design of 6T SRAM cell which offers an advanced approach to low-power and high-speed memory implementation. The circuit consists of 2 cross-coupled inverters formed by CNTFETs and two access transistors controlled by the word line (WL), which link the bit lines (BL and BLB) to the internal storage nodes (Q and QN). Using DG SB CNTFETs enhances current drive, reduces short-channel effects, and allows efficient control of threshold voltages, thereby improving stability and reducing leakage. Simulation results with circuit graphs demonstrate the cell's ability to perform read and write operations reliably, with higher on-currents and reduced power consumption compared to traditional MOSFET-based SRAM designs. The waveforms of Q, QN, BL, BLB, and WL validate correct switching behavior, while supply current plots highlight the transient spikes during write and read operations, confirming the robustness of the DG SB CNTFET-based 6T SRAM cell.

DDC is dual drain contact it is used in CNTFET where two drain terminals are used for better control, performance, or layout optimization in static random access memory cells [13-15].

WL, BL & BLB are Word, Bit Line & Bit Line Bar

WE- Write Enable,

D_{in}- data to be written into the SRAM cell.

V_{DD} & V_{SS} – Power Supply

SE- Sense Enable

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In any SRAM cell, data is stored using cross-coupled inverters, and access to this data is managed through bit lines.

In SRAM cell design BL and BLB are complementary signals used in read/write operations. Which improves speed, reliability, and noise immunity. Also shows significant improvement in stability. In an SRAM array deviating voltage detection amplifiers is also used to reduce layout area, ensures full voltage swing across BL/BLB lines.

V. CONCLUSION

A 6T SRAM cell is design by using double gate SBCNTFET. As DGSBCNTFET is having low leakage current so this proposed structure is very well suited to in the field of low power digital design. It can be clearly shown from table 4 that the design and simulation of 6T-SRAM cell using DGSBCNTFET has far better results as compared to CMOSCNTFET. The analysis is performed using HSPICE simulator for power dissipation and stability. The simulation results provides that the 6T SRAM cell designed using DG-SBCNTFET provides a stable design leads to power reduction as compared to conventional CNTFET. It can be clearly seen from results in table 4 that the proposed model is suitable for low power digital design. Similar static noise margin can be achieve in proposed model with 20% reduced static power dissipation.

REFERENCES

[1] W. Gong et al., Nanomaterials, vol. 15, no. 15, Art. 1168, 2025-The authors discuss CNTFET scaling challenges, leakage mitigation strategies, and related simulation outcomes.

[2] P. Rahul and colleagues, “Improving VLSI efficiency using CNTFET-based designs,” Proceedings of Atlantis Press, 2025.

[3] D. Rhee et al., “Tunable ferroelectric CNT transistors and ternary CAM modeling,” Nature Communications, 2025.

[4] N. Mittal, I. U. Khan, and N. K. Misra, “Tunable nano-CMOS LC ladder filter using Gm-C design,” International Journal of Nano Dimension, vol. 14, no. 3, pp. 238–256, 2023.

[5] M. Radosavljevic, J. Appenzeller, and P. Avouris, “Performance improvements in potassium n-doped CNTFETs,” Applied Physics Letters, vol. 84, pp. 3693–3695, 2024.

[6] K. Alam and R. Lake, “Impact of doping on CNT transistors featuring source/drain underlaps,” IEEE Transactions on Nanotechnology, vol. 6, no. 6, 2007.

[7] D. Peng et al., “CNT materials as promising candidates for future IC technologies,” Materials Today: Nano, Apr. 2024, doi: 10.1016/j.mtnano.2024.01.002.

[8] H. B. K., “Dynamic-GDI-based low-power circuits implemented in CNTFET technology,” ACM, 2024, doi: 10.1145/3611315.3633236.

[9] L.-M. Peng, Z. Zhang, and C. Qiu, “CNT-based digital electronic systems,” Nature Electronics, vol. 2, pp. 499–505, 2019, doi: 10.1038/s41928-019-0330-2.

[10] N. Mittal, I. U. Khan, and Z. H. Khan, “A nano-scaled low-power LPF with enhanced linearity for next-gen WSNs,” International Journal of Nano Dimension, vol. 15, no. 4, pp. 1–2024, doi: 10.57647/j.ijnd.2024.1504.27.

[11] A. Keshavarzi and A. Raychowdhury, “General framework for designing low-power CNTFET multi-valued logic circuits,” IET Computing, vol. 7, no. 2, pp. 95–103, 2019.

[12] I. U. Khan, D. Balodi, and N. K. Misra, “A low-power LC-QVCO with improved phase noise in 0.13-μm RF-CMOS for WLAN systems,” Circuits, Systems, and Signal Processing, vol. 41, no. 5, pp. 2522–2540, 2024.

[13] M. Shulaker et al., “CNT circuit integration at sub-20 nm channel dimensions,” ACS Nano, vol. 8, no. 4, pp. 3434–3443, 2014.

[14] N. Mittal, I. U. Khan, and Z. H. Khan, “WSN-oriented LPF with improved linearity and reduced power,” International Journal of Computing and Digital Systems, vol. 14, no. 1, 2023.

[15] A. Raychowdhury, S. Mukhopadhyay, and K. Roy, “Ballistic-limit CNTFET modeling for circuit applications,” IEEE Nanotechnology Conference, Aug. 2003, pp. 343–346.

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