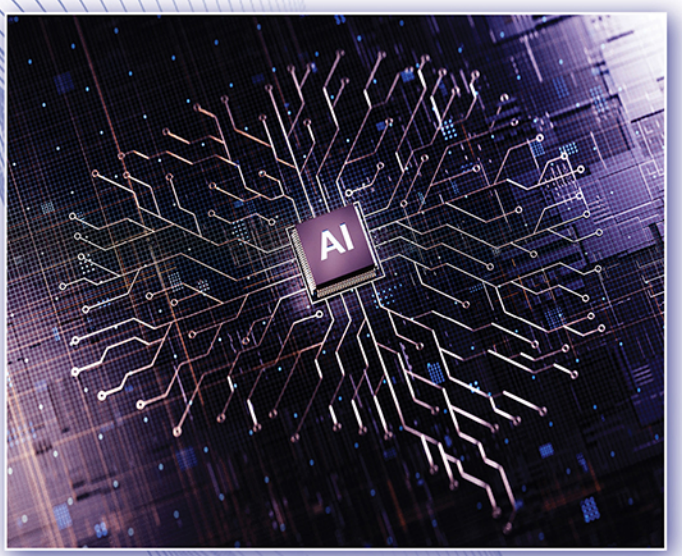
SMART ENGINEERING SYSTEMS

CHIPS AND INTELLIGENCE

LOW POWER VLSI DESIGN WITH ARTIFICIAL INTELLIGENCE



EDITED BY
ABHISHEK KUMAR, SMRITY DWIVEDI, JYOTIRMOY PATHAK, JYOTI KANDPAL AND SUMAN LATA TRIPATHI

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Chips and Intelligence

The text provides a comprehensive and forward-looking exploration of the integration between low-power CMOS VLSI design and cutting-edge technologies such as artificial intelligence and machine learning.

- Explores how artificial intelligence techniques are revolutionizing VLSI design, focusing on optimizing low-power circuits and systems.
- Presents the latest advancements and research in both artificial intelligence and VLSI design, such as FinFET and nanosheet-based logic, analog integrated circuits design, and optimization with artificial intelligence.
- Offers perspectives on future trends and potential developments in the integration of artificial intelligence with VLSI design to reduce the complexity and time-consuming process of semiconductor IC design.
- Addresses techniques for achieving energy efficiency in both digital and analog components and presents future trends in low-power VLSI design.
- Discusses topics such as artificial intelligence-driven adaptive power management in VLSI design and neural networks in low-power VLSI architectures.

The text is primarily written for senior undergraduates, graduate students, and academic researchers in electrical engineering, electronics and communications engineering, microelectronics, VLSI design, artificial intelligence, computer science and engineering.

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Contents

Chapter 5 : Neuromorphic Computing in Low Power CMOS VLSI Circuits

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Abstract: Neuromorphic computing, which attempts to emulate biological neural networks, offers a highly promising way to solve some of the problems with the traditional von Neumann architectures we have known for decades. The chapter explores how some of the principles of neuromorphic computing can be applied to low power CMOS VLSI circuits and spaces to serve the need for pragmatic, energy efficient, high-performance computing systems. Beginning with the concepts of what neuromorphic computing represents and its promise for transforming artificial intelligence and machine learning applications, the chapter continues to look at how to address the design and performance aspects of forming neuromorphic architectures with CMOS technology, including minimizing power consumption, scalability, or performance improvements. The chapter assesses transistor-level approaches to construct the building blocks of neuromorphic computing, including artificial neurons and synapses, all while operating within the restrictions of available CMOS processes. The chapter also looks into some interesting areas, including memristors and phase-change materials for their application into CMOS circuits under neuromorphic computing paradigm. It also examines diving into newer circuit levies and design strategies that emphasize learning and signal processing efficiency perspectives as functionally distributed computational systems. We describe several case study examples of effective CMOS implementations of neuromorphic computing systems, and this chapter suggests types of applications suited for neuromorphic computing in areas including sensory processing and pattern recognition for environments identified as autonomous actors. To sum up, the chapter ends with a discussion of avenues for future research and some anticipated effects of neuromorphic CMOS circuits on next-generation computing paradigms, particularly with regard to ways they might inform the future use of low-power, brain-inspired computing solutions for a variety of uses.

Keywords: Neuromorphic systems; MOS integrated circuits; Sensor networks; Low power electronics; Smart sensors