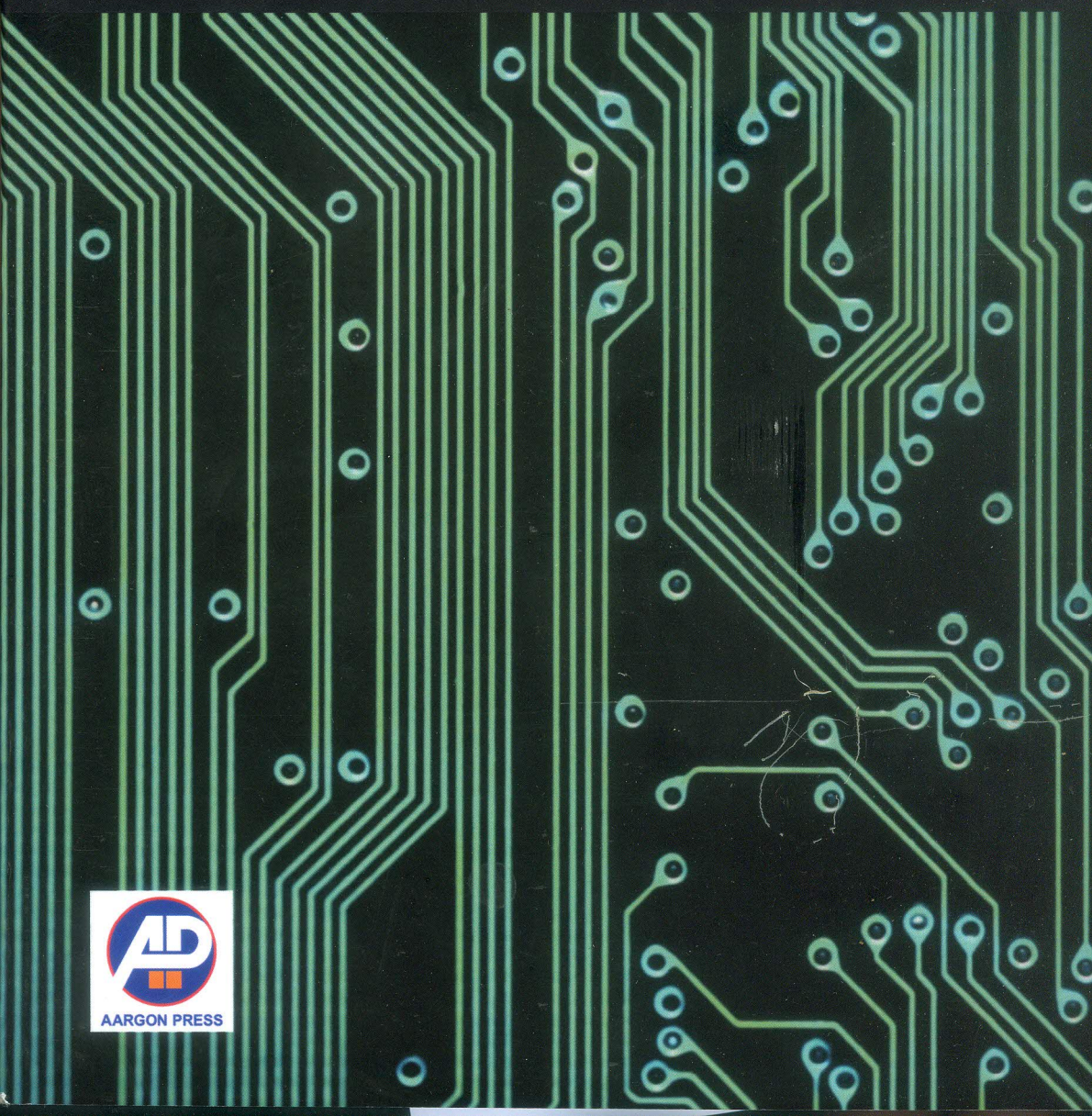
Circuit Design and Signal Processing

N. R. Kidwai
Shailendra Kumar
Mohd Javed Khan



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N. R. Kidwai

Shailendra Kumar

Mohd. Javed Khan

Department of Civil Engineering

Integral University, Lucknow (U.P) INDIA

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CHAPTER 1

Performance Analysis of Fifth Generation Waveform in Rayleigh Fading Environment

Shrish Bajpai, Rajesh

Department of ECE, Integral University, Lucknow (U.P.), India

Multicarrier techniques are gaining more attention to provide larger data rate in future radio communication system. Today the numbers of users are increasing day by day and to provide the best services, more efficiency to users, the more reliable techniques are needed. There are two techniques for modulation, one of them is OFDM. Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier technique which divides the total available bandwidth into subcarriers. It uses the cyclic prefix to reduce the interference between the two or more adjacent carriers and it also makes use of the available bandwidth efficiently. It provides the good spectral efficiency with lower PAPR (Peak to Average Power Ratio). FBMC is a modulation technique which overcomes the various limitations of already existing techniques like PAPR problem in OFDM, intersymbol interference etc. FBMC is a derivative of OFDM. Basically, the FBMC is also a modulation and multiplexing multicarrier scheme and it is used to reduce the interchannel interference in LTE, which is the major problem in the wireless networks and increases the bandwidth efficiency using filter banks to eliminate the interference of the subcarriers instead of using

CHAPTER 2

Design of CORDIC Hardware Efficient Shift-And-Add Algorithm for DSP Processors on FPGA Device using VHDL

Archana Yadav, Mohd Ahmer

Department of ECE, Integral University, Lucknow (U.P.), India

The digital signal processing landscape has long been dominated by the microprocessors with enhancements such as single cycle multiply-accumulate instructions and special addressing modes. While these processors are low cost and offer extreme flexibility, they are often not fast enough for truly demanding DSP tasks. The advent of reconfigurable logic computers permits the higher speeds of dedicated hardware solutions at costs that are competitive with the traditional software approach. Unfortunately algorithms optimized for these microprocessors based systems do not map well into hardware (FPGA). While hardware efficient solutions often exist, the dominance of the software systems has kept these solutions out of the spotlight. Among these hardware-efficient algorithms is a class of iterative solutions for trigonometric and other transcendental functions that use only shifts and adds to perform. The trigonometric functions are based on vector rotations, while other functions such as square root are implemented using an incremental expression of the desired function. The trigonometric algorithm is called CORDIC an acronym for Coordinate Rotation Digital Computer. The incremental functions are performed with a

CHAPTER 3

Implementation of Wide band Frequency Synthesizer Base on DFS (Digital Frequency Synthesizer) controller using VHDL

Archana Yadav, Mohd Amir Rauf

Department of ECE, Integral University, Lucknow (U.P.), India

A frequency synthesizer is an electronic system for generating any of a range of frequencies from a single fixed time base or oscillator. They are found in many modern devices, including radio receivers, mobile telephones, radiotelephones, walkie-talkies, CB radios, satellite receivers, GPS systems, etc. Direct Digital Synchapter (DDS) is a kind of frequency synthesizer that use electronic methods for digitally creating arbitrary waveforms and frequencies from a single, fixed source frequency. Direct Digital Frequency Synchapter (DDFS) is a mixed signal part i.e. it has both digital and analog parts. DDFS's digital part is also known as Numerically Controlled Oscillator (NCO), which consists of a Phase Register, a Phase Accumulator (PA) and a ROM. The analog part has Digital-to-Analog Converter and a filter. NCO is a digital computing block which renders digital word sequences in time at a given reference clock frequency, which thereafter are converted into analog signals to serve as a synthesizer. The phase accumulator (PA) clocked with, generates the phase value sequence. Application of the DDFS ranges from instrumentation to modern communication systems, which employs spread-spectrum and phase shift-keying modulation techniques.

The focus of this paper is on design, analysis and simulation of DDFS, using tools like Xilinx and Modelsim. Traditional designs of high

CHAPTER 4

Study and Performance Analysis of Turbo Coder

Saif Ahmad, Mohd Amir Ansari, Ekta Rai

Department of ECE, Integral University, Lucknow (U.P.), India

In this chapter, turbo encoder is designed using the parallel link of two convolution encoder which is isolated by interleaver. Turbo codes assume in pivotal job in various application for instance portable radio, modernized video, remote satellite correspondence, deep space communication, military application et cetera. Here, simulation of turbo encoder and decoder which is parallel link of recursive precise convolution encoder and interleaver are simulated using MATLAB.

Keywords: Turbo encoder, Turbo codes, and interleaver.

4.1 Introduction

From the last few year we are connected to digital worlds. There has been a proliferation of wireless standards in television, radio and mobile communications. As a result, compatibility issues have emerged in wireless networks. Some of the most popular standards include wireless local area network (WLAN), i.e., IEEE 802.11; 2.5G/3G mobile communications, i.e., Global System for Mobile Communication (GSM), Universal Mobile Telecommunication System (UMTS), Long Term Evolution (LTE); digital television standards, i.e., Digital Video Broadcast (DVB), Advanced Television Systems Committee (ATSC) standards; digital radio standards, i.e., Digital Audio Broadcasting (DAB). The inconsistency between the wireless standards is causing a lot of problems to equipment vendors, network operators and user. Equipment sellers face difficulties in airing new technologies because of short time-to-market requirements. The users are forced to change

CHAPTER 5

MULTIPLE-INPUT FLOATING GATE MOS TRANSISTOR BASED DIFFERENTIAL PAIR DESIGN

M Y Yasin, Nupur Mittal, Shraddha Srivastava

Department of ECE, Integral University, Lucknow (U.P.), India

Downscaling trend of the integrated circuit technology in general and in portable electronics and solar powered systems in particular have considerably increased the demand for low supply circuits and systems. The differential amplifier is widely used as an input stage for operational amplifiers, comparators, operational transconductance amplifiers, analog multipliers and other systems. The folded cascode differential pair topology is used because it is suitable for low- voltage applications. The basic principle for low-voltage operation is to reduce the effective MOS transistor's threshold voltage by connecting one of the control terminals to a supply rail and use remaining terminals for signal-injection. The advantages of using MIFG MOS transistors at the input of the amplifier circuit are the reduction of the power consumption and the increase of the input range since the topology is operating at low voltage. This low voltage differential pair also offers rail-to-rail output voltage swing and hence can be used for any operational amplifier configuration under a variety of circumstances.

Keywords: differential amplifier, MOS transistor's threshold voltage, and MIFG MOS transistors.

5.1 Introduction

Since the development of integrated circuits, the differential pair circuit has been employed as the basic building block in analog and mixed signal circuit design. The increasing demand of portable electronic devices generates a need

CHAPTER 6

Current Mirror Integrator & Analog Signal Processing

M Y Yasin, Saima Beg, Kamini

Department of ECE, Integral University, Lucknow (U.P.), India

The revolving technologies demand of high performance, low voltage (LV) and low power (LP) consumption circuit has forced the research in the direction to work at low voltage supply. These LV circuits have to slow a reduction of power consumption to maintain a longer lifetime. In this area, the obstacles of the voltage mode signal processing techniques such as gain bandwidth product limitation, dynamic range etc. are going to overcome by the current mode approaches. The current mode circuits are utilized as low voltage due to, the current signal is compressed as voltage mode using active devices. The Current Mirror is considered as basic circuit block of the current mode architecture as all the active devices like amplifier, integrator, differentiator etc. can be made by a suitable connection of one or two Current Mirrors (CMs). Moreover, for making current mirrors attractive for portable systems, the low voltage (LV) and low power (LP) ability need to be achieved. For low voltage mode diode connected transistor is used that keeps the transistors always in saturation region. The Current Mirror integrator is an important circuit block, which is widely used in analog signal processing applications such as filter designs, waveform shaping process controller design calibration circuit etc.

Keywords: Current Mirrors, DSP and ASP.

6.1 Introduction

Signal processing is an operation that changes the characteristics of a signal and these characteristic include amplitude, shape, frequency and phase content

CHAPTER 7

Performance Analysis of Dual Hop Amplify and Forward Relaying Over Time Varying Fading Channel

Dharmendra, Qazi Saeed Ahmad

Department of Civil Engineering, Integral University, Lucknow (U.P.), India

In this chapter a joint relay and antenna selection scheme is proposed and implemented. This scheme consists of M relays in multiple FD relay networks and a source and destination node. An antenna selection procedure is explained in detail where, the optimal relay with the best transmitter- receiver configuration was chosen to carry out communication between the source and the destination node. Closed form expressions for CDF, Antenna Selection Method, Outage Probability and SER were derived and the evaluation of their results was achieved. Simulations were obtained for Outage Probability has been shown in the project demonstration. An analysis of the results has been carried out in the same section through a comparison of the proposed system with a conventional system. Through the implementation of the project, we have achieved additional space diversity at the destination node which has resulted in better performance in comparison to the ORS system. This additional space diversity was achieved in the ARS method because of a trade off with SI. A permissible amount of SI was allowed to affect the system at the cost of increasing space diversity through intelligent antenna and relay selection. The system still suffers from the effects of deep fading on the channel link between the relay, source and destination nodes. Outage Probability reaches high values as the value of SNR increases and analysis of the system could not be achieved at these values. This arises due to self-interference at the relay node. The performance of the system can be better improved by implementing better self-interference cancellation methods at the relay node in future work.

Keywords: Relaying, ORS and Hop.

CHAPTER 8

Design and Characterization of 16 Bit Multiplier Accumulator Based On Radix-2 Modified Booth Algorithm

Imran Ullah Khan, Vijay Dhar Maurya
Department of ECE, Integral University, Lucknow (U.P.), India

This chapter is all about to implementation of Multiplier-and-accumulator (MAC) for high-speed arithmetic. By combining multiplication with accumulation and devising a hybrid type of carry save adder (CSA), the performance was improved. Since the accumulator that has the largest delay in MAC was merged into CSA, the overall performance was raised. The proposed CSA tree uses 1's complement-based radix-2 modified Booth's algorithm (MBA) and has the modified array for the sign extension in order to escalation the bit density of the operands. The CSA propagates the carries to the least significant bits of the partial products and generates the least significant bits in advance to decrease the number of the input bits of the final adder. Also, the proposed MAC accumulates the intermediate results in the type of sum and carries bits instead of the output of the final adder, which made it possible to optimize the pipeline scheme to improve the performance. Based on the theoretical and experimental estimation, we analyzed the results such as the amount of hardware resources, delay, and pipelining scheme.

Keywords: Multiplier, Accumulator, MAC & CSA.

8.1 Introduction

The ongoing quick advances in multimedia and communication systems,

CHAPTER 9

Optimization of Intelligent Spectrum Sensing Techniques for Cognitive Radio Networks

Qazi Saeed Ahmad, Imran Ullah Khan, Rizwan Ahmad

Department of ECE, Integral University, Lucknow (U.P.), India

In this chapter we have compared the accuracy and performance of cognitive radio (CR) networks in three various techniques energy detection, matched filter and the Cyclostationary detection by using various such as time, cost and complexity. It has been found that the performance and accuracy are relying on what extent availability of the prior knowledge for PU signal. Further the complexity also increased when spectrum sensing techniques require more prior knowledge to detect PU. In contrast increasing knowledge caused high cost and takes long time. Sensing scheme namely was projected to improve the usage efficiency of the radio spectrum by increasing detection reliability and decreasing sensing time. This chapter investigates some of the major aspects and challenges involved in CR networks; however, we have just scratched the surface concerning this new communication paradigm. Therefore, we need specific technique which might be answered in future work by combining the perfect features by using two techniques whereby possesses minimum prior knowledge of the PU, low cost, short time and low complexity.

Keywords: Cognitive, Radio, Networks & Spectrum.

9.1 Introduction

Spectrum allocation typically happens through a licensing process. However,

CHAPTER 10

Proton irradiation study of HfO_2, a high-K dielectric

Saima Beg, Savita Maurya, Supriya Awasthi

Department of ECE, Integral University, Lucknow (U.P.), India

In this world of technology, with regular updates, the life without electronic devices is unbelievable. As to provide better technology in terms of speed, power–loss and cost, the components of these electronic devices are 'scaled' down in size in order to achieve higher device density and faster switching speed and because of this kind of aggressive scaling IC's (Integrated Circuits) requires continuous miniaturization of the MOS (Metal Oxide Semiconductor) Transistor structure, includes thickness of gate dielectric. This has resulted to some conventional limitations of silicon dioxide (SiO_2) such as undesirable leakage current, uniformity control, and reliability requirements. SiO_2 becomes so thin that tunneling of charge carriers takes place. Researchers have used some alternative materials with higher dielectric constant than that of SiO_2 to replace the long existing SiO_2. In this work, hafnium dioxide based MOS Capacitors have been used as a sample for further study. Atomic layer deposition was used to deposit hafnium dioxide. Electrical (C-V, G-V, and I-V) measurements were taken before and after irradiation with 2.7 MeV protons. To quantify the quality of deposited oxide and further the effect of radiation, C-V and G-V measurements were taken at different frequencies 1 kHz, 10 kHz, 100 kHz, 200 kHz, and 500 kHz and 1 MHz at room temperature.

Keywords: irradiation, dielectric & Nano-scale.