Dissertation

on

Performance Analysis and characterization of Dual-Material Double Gate Metal Oxide Semiconductor Field Effect Transistor

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in

Electronic Circuits and Systems

Submitted By:

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UNDERTAKING FROM THE CANDIDATE

This is to certify that I Yusra Siddiqui have completed the M.Tech Dissertation work on the topic **"Performance Analysis and characterization of Dual-Material Double Gate Metal Oxide Semiconductor Field Effect Transistor"** under the supervision of Mrs. Nupur Mittal for the partial fulfillment of the requirement for the Master of Technology (M.Tech.) in Electronic Circuits and Systems from Department of Electronics and Communication Engineering, Integral University, Lucknow. This is an original piece of work &I have not submitted it earlier elsewhere.

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ACKNOWLEDGEMENT

"He is the source of all light and His light is diffused throughout the universe God has given the man intelligent speech, power of expression, and capacity to understand clearly the relations of things."

We are living in the age of electronics and this field has witnessed radical changes over the last decades. We have observed vast application of electronics in almost every walk of life especially in the field of medical science. This fascinated me to do something in this field as a student of electronics science.

Every accomplishment entails the endeavor of many people and this work is no atypical. Today, I carpe diem to thank them all. First and foremost, I would thank the Almighty whose infinite grace makes all things possible. I am grateful to my parents who have inculcated in me good values and culture, and my husband for his constant support and understanding. This work is dedicated to them as a token of love.

Due to the contribution of time and effort by many people, this project could reach a conclusion. I feel great pleasure in expressing my sense of gratitude and sincere thanks to my project guide Mrs. Nupur Mittal and Co Guide Dr Imran Ullah Khan, Department of Electronics and Communication Engineering for their consistent and careful guidance throughout this project work. I felt proud to get the opportunity to work under them, which has enlightened my thoughts and enriched my experience. I am grateful to Dr Syed Hasan Saeed, Professor and Head, Department of Electronics and Communication Engineering for providing necessary facilities in the department. I am also thankful to Dr Shailendra Kumar for his constant support and encouragement throughout this project.
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ABSTRACT

This work describes the evolution of the SOI MOSFET from single-gate structures to double-gate and gate-all-around structures. Increasing the "effective number of gates" improves the electrostatic control of the channel by the gate and, hence, reduces short-channel effects. Due to the very small dimensions of the devices, one-and two-dimensional confinement effects are observed, which results in the need of developing quantum modelling tools for accurate prediction of the electrical characteristics of the devices. This work is divided into the, a quick review in some important issues as SOI technology and the advantages over bulk-Si technology, MOSFET devices and how they operate, Short channel effects, Multi-Gate devices and scaling limits of those devices. Also mention nine of the most important and frequently used experimental extraction methods of threshold voltage. Those nine methods, include: the constant current (CC) method, the extrapolation in the linear region (ELR) method, the transconductance linear extrapolation (GMLE) method, the second derivative (SD) method, the ratio method (RM), the second derivative logarithmic (SDL) method, the critical-current at linear-threshold (I_{crit} at V_{TO}) method (combination of CC method with SD method), the critical-current at linear-threshold (I_{crit} at V_{TO}) method (combination of CC method with GMLE method), and the maximum-$d(g_m/I_D)/dV$g method. In the next two Sections, we will first take a quick view on the analytical expressions of the potential distributions of a double-gate (DG) and then an analytical unified model for the threshold voltage V_T of double-gate is proposed.

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LIST OF ABBREVIATION

Abbreviation	Name
ANN	Artificial Neural Network
BOX	Buried Oxide
CMOS	Complementary Metal Oxide Semiconductor
DG	Double Gate
DIBL	Drain Induced Barrier Lowering
DM	Dual Material
DRAM	Dynamic Random Access Memory
FD	Fully Depleted
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSE	Mean Square Error
nMOS	n-channel Metal Oxide Semiconductor
PDF	Probability Density Function
pMOS	p-channel Metal Oxide Semiconductor
RF	Radio Frequency
SCE	Short Channel Effects
Si	Silicon
SIMOX	Separated by Implanted Oxygen
SiO_2	Silicon dioxide
SM	Single Material
SOC	System On Chip
SOI	Silicon-On-Insulator

CHAPTER 1

INTRODUCTION

1.1 Modern Day Scenario of VLSI Domain

The cost of design, manufacture, and test of modern-day VLSI chips is increasing so rapidly that the semiconductor industry is treading cautiously when adopting new technologies. As per Moore's law, the device density doubles every 1.5 years, which amounts to a Compound Annual Growth Rate (CAGR) of 59%. The ITRS report of 1999 pointed out the gap between this growth rate and the rate at which design productivity has been increasing (~25% CAGR) over the years [1]. Design productivity is measured in terms of the number of transistors that can be designed per staff-month. Software productivity has been growing at an even slower rate of 10%.

1.2 Scope and classification of the MOSFET

The applications of MOSFET are [2]

- Amplifiers made of MOSFET are extremely employed in extensive frequency applications.
- The regulations for DC motors are provided by these devices.
- As because these have enhanced switching speeds, it acts as perfect for the construction of chopper amplifiers.
- Functions as a passive component for various electronic elements.
- In the end, it can be concluded that the transistor requires current whereas MOSFET requires a voltage. The driving requirement for the MOSFET is much better, much simpler as compared to a BJT.

1.2.1 Basics of MOSFET

The MOSFET is an important element in embedded system design which is used to control the loads as per the requirement. Many of electronic projects developed using MOSFET such as light intensity control, motor control and max generator applications. The MOSFET is a high voltage controlling device provides some key features for circuit designers in terms of their overall performance. This article provides information about different types of MOSFET applications.

1.2.2 MOSFET and Its Applications

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices. The MOSFET is a three terminal device such as source, gate, and drain [3]. The MOSFET is very far the most common transistor and can be used in both analog and digital circuit.

The MOSFET works by varying the width of a channel along which charge carriers flow (holes and electrons). The charge carriers enter the channel from the source and exits through the drain. The channel width is controlled by the voltage on an electrode is called gate which is located between the source and drain. It is insulated from the channel near an extremely thin layer of metal oxide. There is a different type of MOSFET applications which is used as per the requirement.

1.2.3 Types of MOSFET Devices

The MOSFET is classified into two types such as;

- Depletion mode MOSFET
- Enhancement mode MOSFET

Depletion Mode

When there is zero voltage on the gate terminal, the channel shows its maximum conductance.

Figure 1.1 : Depletion mode MOSFET [1]

As the voltage on the gate is negative or positive, then decreases the channel conductivity. Depletion mode MOSFET is shown in figure 1.1.

Enhancement Mode

When there is no voltage on the gate terminal the device does not conduct. More voltage applied on the gate terminal, the device has good conductivity. Enhancement mode MOSFET is shown in figure 1.2.

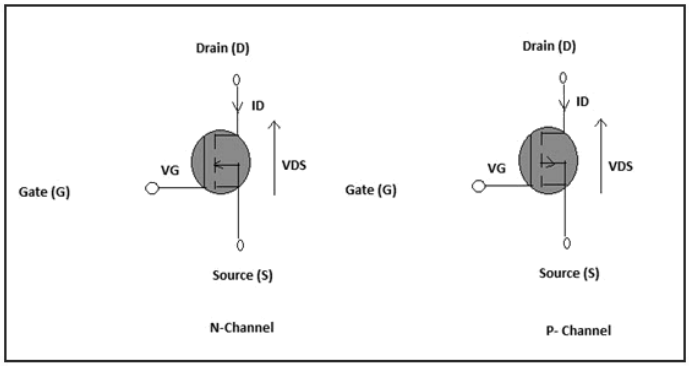


Figure 1.2 : Enhancement Mode MOSFET [1]

1.2.4 MOSFET Working Principle

The working of MOSFET depends upon the metal oxide capacitor (MOS) that is the main part of the MOSFET. The oxide layer presents among the source and drain terminal. It can be set from p-type to n-type by applying positive or negative gate voltages respectively. When apply the positive gate voltage the holes present under the oxide layer with a repulsive force and holes are pushed downward through the substrate. The deflection region populated by the bound negative charges which are allied with the acceptor atoms.

1.3 Basics of Double Gate Structures

Different gate structures and a bulk device are discussed, also how the electric field lines propagate through the depletion regions associated with the junctions.

1.3.1 Different Gate Structures

Different gate structures are shown in figure 1.3. In a bulk device shown in figure 1.4.A, the electric field lines propagate through the depletion regions associated with the junctions. Their influence on the channel can be reduced by increasing the doping concentration in the channel region. In very small devices, the doping concentration becomes too high (10^{19} cm^{-3}) for proper device operation, unfortunately. In a fully depleted SOI (FDSOI) device, most of the field lines propagate through the buried oxide (BOX) before reaching the channel region shown in figure 1.4.B. Short-channel effects can be reduced in FDSOI MOSFETs by using a thin buried oxide and an underlying ground plane. This approach, however, has the inconvenience of increased junction capacitance and body effect [6]. A much more efficient device configuration is obtained by using the double-gate transistor structure.

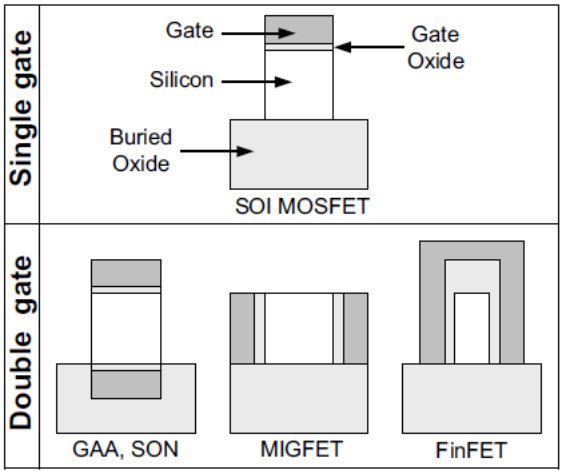


Figure 1.3: Different gate structures [2]

The electric field lines from source and drain underneath the device terminate on the bottom gate electrode and cannot, therefore, reach the channel region shown in Figure 1.4 C. Double gate MOSFET is shown in Figure 1.4 D.

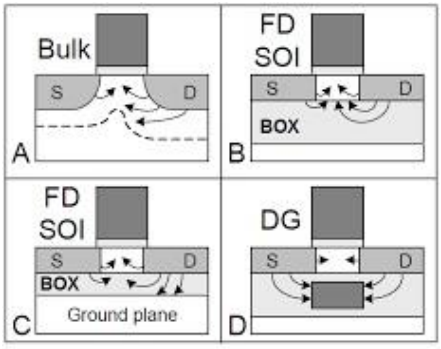


Figure 1.4 : Encroachment of electric field lines from source and drain on the channel region in different types of MOSFETs: A) Bulk MOSFET, B) Fully depleted SOI MOSFET, C) Fully depleted SOI MOSFET with thin buried oxide and ground plane, D) Double-gate MOSFET [4]

1.3.2 Multi-Gate MOSFET Devices

The most promising technology today for the control of short channel effects is multi-gate MOSFETs. While it is not a new idea and originates from early 60s, the need for the suppression of SCEs towards the continuous scaling of electronic devices brought them up to the surface the last years. The adjacent figure shows cross sections of different types of multi-gate devices as have been proposed lately. The multiple advantages of multi-gateMOSFETs can be summarized in the following points.

- Electrostatic shielding of the channel from parasitic electric fields originating from the gates and the drain. The mobility is increasing while the transverse electric fields cannot penetrate inside the channel.
- Better control of the channel because of the gates coupling. Better subthreshold slope and smaller DIBL parameter are obtained.
- Two or more inversion volumes are created, that result in higher on-current and faster carrier transport within the tiny volume of the channel film.

The most promising and closer-to-application devices today are double-gate and tri-gate FinFETs, due to their superior scalability and ease of fabrication processing. The first article on the double-gate MOS (DGMOS) transistor was published by T. Sekigawa and Y. Hayashi. That paper shows that one can obtain significant reduction of short- channel effects by

sandwiching a fully depleted SOI device between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter Ξ (*Xi*). The first fabricated double-gate SOI MOSFET was the "fully Depleted Lean-channel TrAnsistor (DELTA)", where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin". The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin. The hard mask is used to prevent the formation of parasitic inversion channels at the top corners of the device. Other implementations of vertical-channel, double-gate SOI MOSFETs include the "Gate-All-Around device" (GAA), the Multi-Fin XMOS (MFXMOS), the triangular-wire SOI MOSFET and the Δ-channel SOI MOSFET.

The triple-gate MOSFET is a thin-film, narrow silicon island with a gate on three of its sides. Implementations include the quantum-wire SOI MOSFET and the tri-gate MOSFET. The Electrostatic Integrity of triple-gate MOSFETs can be improved by extending the sidewall portions of the gate electrode to some depth in the buried oxide and underneath the channel region (Π-gate device and Ω-gate device). From an electrostatic point of view, the Π-gate and Ω-gate MOSFETs have an effective number of gates between three and four.

The structure that theoretically offers the best possible control of the channel region by the gate, and hence the best possible Electrostatic Integrity is the surrounding-gate MOSFET. The first surrounding-gate MOSFETs were fabricated by wrapping a gate electrode around a vertical silicon pillar. Such devices include the CYNTHIA device (circular-section device) and the pillar surrounding-gate MOSFET (square-section device). More recently, planar surrounding-gate devices with square or circular cross sections have reported. To increase the current drive per unit area, multiple surrounding-gate channels can be stacked on top of one another, while sharing common gate, source and drain. Such devices are called the Multi-Bridge Channel MOSFET (MBCFET), the Twin-Silicon-Nanowire MOSFET (TSNWFET), or the Nano-Beam Stacked Channels (GAA) MOSFET [7-10].

1.3.3 Double-Gate FD SOI MOSFETs

Double-gate SOI MOSFET has two gates simultaneously controlling the charge in the thin silicon body layer, allowing for two channels for current flow. Because SOI film is thin, a direct charge coupling exists between the front and back gate invariably [11], influencing the terminal characteristics of the device. The device can be operated in several ways [12]:

- Front channel alone conducting, the back channel being either depleted oraccumulated.
- Both channels conducting, both or either of the channels being in weak or stronginversion.

The current-voltage characteristics of the device with the front channel in strong inversion and the back channel either in accumulation or in depletion has been modeled analytically. Since SOI films are thin, the electrical properties of MOSFETs fabricated are inherently influenced by the charge coupling between the front and back gates. Due to extremely small device dimensions, low voltage operation will be mandatory where the low threshold voltage is required [12].

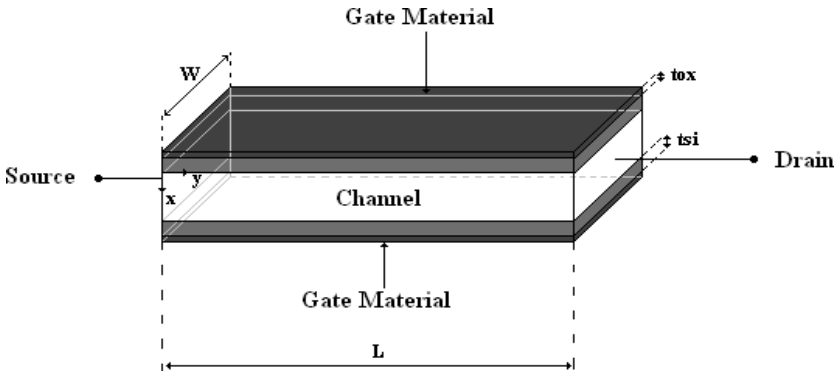
The requirement of low voltage operation made the investigations of subthreshold characterization important. The subthreshold behavior of a MOSFET is characterized by the subthreshold swing, which has to be small enough to ensure low leakage current and sufficient overdrive necessary for high speed. The dependence of the subthreshold swing (S-factor)* on current capability of the MOSFET has been discussed for the gate length down to 0.1 μm [12]. In the subthreshold region, the floating body (of FD SOI device).

1.3.4 Threshold Voltage Model of an Undoped Symmetric DG FinFET

A Double gate (DG) MOSFET is considered to be the best candidate for device downscaling, as it allows significant reduction of the short-channel effects (SCEs), such as threshold voltage roll-off, drain-induced barrier lowering (DIBL) and subthreshold slope degradation [11-13]. Moreover, intrinsic or lightly doped channel is preferred as such devices possess advantages, such as absence of dopant fluctuation which contributes to variations of the threshold voltage and drive current and enhanced carrier mobility owing to the absence of depletion charges which can contribute to the effective electric field, thus degrading the mobility.

To develop a physical model for extremely scaled DG MOSFETs, the potential distribution throughout the tiny volume of the silicon film must be accurately determined under the application of gate and drain bias voltages. However, compared to a single-gate structure, in DG MOSFETs, the coupling between the gates changes completely the form of the potential distribution within the tiny volume of the silicon channel. More specifically, because of the symmetrical device structure, the potential is increased, exhibiting a maximum at the middle of the silicon body.

According to Andreas Tsormpatzoglou et. al., three main approaches need to be considered to obtain an analytical expression of the potential distribution along the channel of DG MOSFET [13]. The first approach is based on the strong assumption that the potential within the channel $\Phi(x, y)$ can be written as $\Phi(x, y) = \Phi(x) \cdot \Phi(y)$, and then, the Poisson equation is solved for every axis. The solutions of the partial differential equations, with the proper boundary conditions, can be written as Fourier series but this leads to complicated expressions, which need high-class series coefficients to achieve good agreement between numerical solution and analytical expressions. The second approach uses the Gauss' law, where special parameters must be introduced to describe the change of the electric potential along the vertical axis. The solutions can describe adequately the potential distribution along the channel only at the front and back gate interfaces. Finally, in the third approach, a solution is obtained using Poisson's equation and a parabolic function for the electric potential along the vertical dimension, describing the potential distribution only at the front and back gate interfaces.



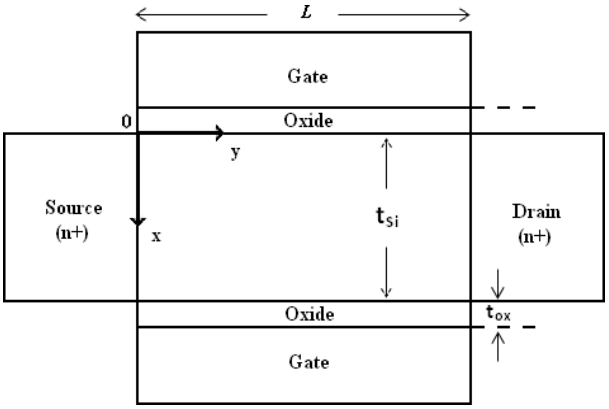


Figure 1.5 : Schematic cross section of a symmetric planar DG MOSFET [3]

1.4 Si MOSFET and SOI MOSFET

As the device count in an IC is running into billons per chip, the issue of power dissipation in the chip is becoming one of the two most important issues (other being the speed). The ever decreasing device dimensions have reached a state where the performance of the bulk Si MOSFETs is limited by the fundamental physical limits such as reduction in carrier mobility due to impurities, increasing gate tunneling effect as the gate oxide thickness decreases and increasing p-n junction leakage current as the junctions become more and more shallow. A low operating voltage is a necessity as reduced power consumption is aimed at. These requirements have led to development of alternative technologies. SOI technology is one such alternative which can offer a performance as expected from next generation Si technology.

Figure 1.6 shows the structures of n-enhancement bulk Si MOSFET and the corresponding SOI MOSFET. The main difference between the two is that the in SOI structure the Si layer containing the MOSFET is separated from the substrate by a layer ofSiO_2, called buried oxide (BOX). The thin Si film on BOX is a crystalline layer. The typical dimensions of the layers are shown in the figure 1.6.

1.4.1 Operating Modes of SOI MOSFETs

There are two operating modes of partially-depleted (PD) vs fully-depleted (FD).

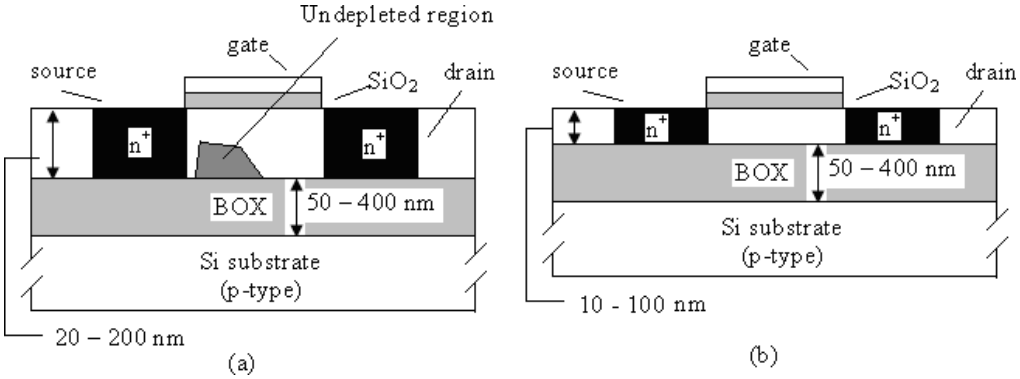


Figure 1.6 : n-enhancement bulk (a) Si and (b) SOI MOSFET [13]

In PD MOSFET, a part of the body region remains undepleted or neutral while in FD MOSFET, whole of the body, the depletion region extends right up-to the body and BOX interface. Thus in FD SOI MOSFET, the complete body region is depleted off majority carriers.

1.4.2 Comparison of PD and FD SOI MOSFETs

The characteristics of PD and FDMOSFETs differ in the following respects [12].

Kink in the drain current characteristics

In PD SOI MOSFETs, a kink (sharp rise in drain current at a particular drain voltage) is observed in the I_D vs V_{DS} characteristics as the drain voltage is increased for a fixed gate voltage. As in n-channel MOSFETs as the electrons flow towards the drain they gain kinetic energy and generate electron-hole pairs by impact-ionization. The holes so generated moves towards the source. In PD SOI device there is higher potential barrier to the holes so the hole tend to accumulate in the body region thereby increasing the body voltage. This causes threshold voltage to drop, drain current to increase leading to even higher impact-ionization. At the same time barrier height for holes also decreases permitting more number of holes to reach the source thereby increasing the drain current. This results in sharp increase in the drain current (a kink) at some drain voltage. To avoid this kink the body of PD SOI MOSFETs needs to be connected to ground. In FD SOI devices, the potential barrier to the hole at the source end is small because whole of the body region is depleted of the carriers. So, there is no

accumulation of holes in the body region and consequent kink in the drain characteristics.

Subthreshold Slope

An important feature of FD SOI MOSFET is that they have steep subthreshold behavior characterizes by subthreshold swing close to 60 mV/decade which is limiting value for MOSFETs. The subthreshold behavior of PD SOI is similar to bulk Si MOSFETs. Thus subthreshold characteristics of FD SOI MOSFETs are superior.

Dynamic Floating Body Effects

As mentioned above, the SOI devices are fully isolated and their body potential is not constant. The effects of different bodypotential are collectively known as floating body effect. Dynamic body floating effectsrefer to the device behavior when it is operating in a circuit. The body potential changesbecause of impact-ionization in majority redistribution in the body region when gate anddrain switch between high and low levels. FD SOI devices are stable and relativelyunaffected by the dynamic body effects. In contrast the PD SOI devices are significantlysensitive to dynamic body effect and require the body to be connected to a constantpotential. These floating body effects have been known to cause the transientphenomenon in the access transistor of DRAMs and SRAMs that can lead to loss of chargein memory cell [11].

Parasitic Bipolar Effects

In FD SOI MOSFET, a parasitic bipolar transistor is formed where source, body and drain act as emitter, base and collectorrespectively of parasitic transistor. In this transistor, base current is consist of majoritycarriers, generated by impact-ionization. Since the body region is more depleted in FDthan PD SOI device. The parasitic transistor is more effective in FD SOI devices. Thistransistor leads to a reduction to breakdown voltage between the source and drain,smaller threshold voltage and abnormally steep subthreshold behavior. This parasiticeffect may also lead to single transistor latch phenomenon [12]. The parasitic bipolareffect can be suppressed by suppressing the generation of majority carrier by impact-ionization,

reducing the injection efficiency of the parasitic bipolar transistor and bylowering the transport efficiency in the base of the transistor.

Self Heating Effect

Self heating effects are common to both PD and FD SOI devices. The BOX layer which leads to better characteristic of the device is also responsible for its poor thermal behavior. The oxide has a thermal conductivity which is two orders of magnitude smaller than that of silicon. So, the heat generated by the drain current is not able to escape through the BOX layer and has to be dissipated by the interconnections via the contact of source, drain and gate. This may results in increase in channel temperature and consequent degradation device behavior. have relatively smaller short channel effects, so the gate length can be as small as twice the thickness of SOI layer. Double-gate structures with one gate consisting of dual- material [13] have also been analyzed. Both gates consisting of dual material have been proposed. Triple-gate devices give somewhat better characteristics because three-gates allow better control of channel potential. Gate all around devices have more complicated structure and are difficult to fabricate. FinFET, double and triple-gate are more promising alternatives for nano-scale devices.

1.5 REPORT ORGANIZATION

The report has been divided into five chapters as below:

Chapter 1 includes introduction of metal oxide semiconductor field effect transistor and double gate MOSFET devices.

Chapter 2 Emphasize on Literature survey to the related work.

Chapter 3 This chapter describe, 2D analytical model for potential distribution, electric field distribution, electron velocity distribution and subthreshold swing in n-channel DM DG FD SOI MOSFET is presented. In the analysis, the drain induced barrier lowering (DIBL) has been taken into account.

Chapter 4 In this Chapter, the same has been done for the device parameter: threshold voltage (V_{th}), device capacitance (C_T), drain current characteristics (I_{DS}), transconductance (g_m), drain-resistance (r_{ds}), cut-off Frequency (f_c) and transit time (τ). The analysis of noise behavior of the proposed device has also been presented.

Chapter 5 represents overall results and conclusion.

CHAPTER 2

LITERATURE SURVEY

Literature Survey

This chapter summarize literature survey of metal oxide semiconductor field effect transistor, multi gate structure MOSFET devices including double Gate, Gate all around and double gate, gate all around nanowire devices.

Y. Zhang et al. [1] have proposed a novel Core–Insulator Gate-All-Around (CIGAA) nanowire has been proposed, investigated, and simulated comprehensively and systematically based on 3D numerical simulation. Comparisons are carried out between GAA and CIGAA. The new CIGAA structure exhibits low off-state current compares to that of GAA, making it a suitable candidate of future low-power and energy-efficient devices. The device performance of our proposed CIGAA nanowire using 3D TCAD simulation. Due to CIGAA's lowered off-state current enabled by Core–Insulator, it shows high on-state current, low off-state current, low subthreshold swing, and high switching ratio. CIGAA has the potential to be used to fabricate low-power systems. Thus, the CIGAA nanowire is a promising candidate to extend CMOS scaling roadmap and future low power CMOS devices.

Kosmani N.F. et al. [2] suggested simulation work is to compare the performance of GAA nanowire and DG MOSFET and then study the effect of physical parameter on electrical behavior for both devices. The result of the simulated model of Gate-All-Around nanowire is compared with published data. It was found that when the gate length of DG was scaled from 80nm to 10nm, the subthreshold slope is increasing from 62mV/dec to 162.7mV/dec. While for GAA, the subthreshold slope is increasing from 65.8mV/dec to 127mV/dec. The threshold voltage in DG and GAA at Lg=80nm are 0.40646V and -0.17505V respectively. Even though heavy doping was good for suppressing SCE, the lower doping concentration is desirable as the DG and GAA nanowire had higher on-state currents with 1.42x10-3A and 3.23x10-4A respectively. It also showed that the threshold voltage of DG and GAA nanowire increase from -0.0734V to 0.2312V and -0.0319V to 0.2232V respectively when the channel doping is varies from lower to higher concentration.

Jena, B et al. [3] exploited the a new conical surrounding gate metal-oxide-semiconductor field effect transistor (MOSFET) with triple-material gate has been proposed and verified using TCAD device simulator from Synopsis. The electrostatic performance of conical model with different tapering ratios is extensively investigated and compared with that of cylindrical model (tapering ratio TR = 1). The present model exhibits improved electrostatic behavior for an optimized tapering ratio of 0.98 as compared to the conventional cylindrical model. The results reveal that the triplematerial conical model provides better ON current performance, transconductance and reduced threshold voltage. On the contrary the single-material conical model exhibits maximum ION/IOFF ratio, minimum OFF current and reduced subthreshold swing (SS) in comparison to other models. Thus, the conical model with optimized tapering ratio can be a possible replacement of cylindrical model for low-power and high speed application.

Pal A. et al. [4] extend the use of a 2D analytical model for the Dual Material Surrounding Gate MOSFET (DMSG) by solving the Poisson equation has been proposed and verified using ATLAS TCAD device simulator. Analytical modeling of parameters like threshold voltage, surface potential and Electric field distribution is developed using parabolic approximation method. A comparative study of the SCEs for DMSG and SMSG device structures of same dimensions has been carried out. Result reveals that DMSG MOSFET provides higher efficacy to prevent short-channel effects (SCEs) as compared to a conventional SMSG MOSFET due to the presence of the perceivable step in the surface potential profile which effectively screen the drain potential variation in the source side of the channel. A nice agreement between the results obtained from the model and the results obtained from numerical TCAD device simulator provides the validity and correctness of the developed model.

Islam M.J. et al. [5] used the cylindrical gate-all-around (CGAA) FET (field-effect transistor) structure with Indium Arsenide (InAs) nanowire is used as channel instead of silicon nanowire, and aluminium oxide is used as the gate dielectrics instead of silicon dioxide. The performance of this setup was demonstrated using ATLAS simulator of Silvaco TCAD software. Indium Arsenide is chosen due to its high electron velocity, high saturation velocity and low contact resistance, whereas, aluminium oxide is chosen because of its higher permittivity.

Simulation results indicate that the proposed combination is superior to the CGAA structures having channel-gate dielectrics that use combinations of silicon-silicon dioxide and Indium Arsenide-silicon dioxide. The effects of variation of nanowire radius, channel length and oxide thickness on the output and transfer characteristics curves, and also on the performance parameters such as maximum drain current, maximum transconductance, on resistance and inverse subthreshold slope are investigated to show the superiority of the proposed structure.

Sasaki T. et al. [6] studied the variations in the threshold voltage of *SOS* (silicon on sapphire) *MOSFET* as a function of epitaxial film thickness. Worly derived an analytical model for the threshold voltage of an *SOS* transistor in which charge coupling between the front and theback gates occurs as in *SOI MOSFET*, but only the back silicon surface is depleted.

Sano et al. [7] developed a rigorous numerical model for threshold voltage *(V_{th})* that includes a dependence on the back gate bias. A general steady state analysis of charge coupling between the front and back gate that yielded closed form expressions for V_{th} under all possible steady state charge conditions was presented. They also discussed the dependence of the linear region channel conductance on the back gate bias and other device parameters. Both *n*-type and *p*-type *SOI MOSFET* structures were considered. They analyzed the effect of the interface parameters on the back and the front threshold voltages. The temperature dependence of the threshold voltage of the ultra thin *SOI n*-channel *MOSFET*. The threshold voltage variation with temperature is significantly smaller in fully depleted devices than in bulk devices. In this paper, the dependence of V_{th} on the depletion level was also discussed.

Chen L. et al. [8] the statistical variation of V_{th} resulting from the randomness in impurity distribution in both bulk and SOI MOSFET was discussed. Their study revealed that the thresholdvoltage of DG FD SOI MOSFET is less sensitive to inherent fluctuations in impurity distribution and discussed the design considerations for minimizing the statistical variation in V_{th}. Over the past thirty years, the primary challenge for the IC designers has been the integration of an ever increasing number of devices with high yield and reliability.

However, as the device dimensions approach deep submicron regime, the characteristics of a conventional MOSFET approach that of a resistor. Increasing the threshold voltage through increased channel doping solves this difficulty. However, this would require higher supply voltage and also result in higher capacitance. This combination would result in higher power dissipation and low speed which are undesirable. So a tradeoff is required.

Yan et al. [9] has proposed the guidelines for the design of SOI MOSFETs. They discussed several structural variations of conventional SOI structure in terms of natural length scale to guide the design. The requirement of low voltage operation made the investigations of subthreshold characterization important. The subthreshold behavior of a MOSFET is characterized by the subthreshold swing, which has to be small enough to ensure low leakage current and sufficient overdrive necessary for high speed. The dependence of the subthreshold swing (**S**-factor)* on current capability of the MOSFET has been discussed for the gate length down to 0.1 μm. In the subthreshold region, the floating body (of FD SOI device) leads to a shift in the subthreshold slope which is smaller than the theoretical value of 60 mV / decade predicted for an ideal MOS transistor at room temperature.

Davis et al. [10] observed subthreshold slope as small as 50 mV / decade for n-channel MOSFETs fabricated on SOI substrate. Advances in SOI wafer technology have improved thematerial quality substantially leading to n-channel MOSFET subthreshold slope of less than 20 mV / decade. Good understanding of this subthreshold behavior of floating body SOI MOSFET is necessary for proper transistor design and circuit modeling. Previously reported **S**-factor models are based on one-dimensional analysis of the SOI MOSFET and cannot be applied to short channel devices where the potential distribution is essentially two dimensional. Two-dimensional analysis of subthreshold behavior using numerical analysis approach has been reported in for DG FD SOI devices.

Matloubian et al. [11] showed that n-channel SOI MOSFETs with floating bodies show a threshold voltage shift and improvement in subthreshold slope at higher drain biases.

This improvement was supported by the positive feedback between the body potential and the transistor channel current. Subthreshold slopes in submicron n-channel fully depleted silicon on insulator MOSFETs have been measured as a function of substrate bias and temperature as well as drain bias. It was found that for low drain voltage, a simple capacitor model could explain the experimental results. For large drain voltages anomalously sharp subthreshold characteristics was observed for large negative substrate biases. They also proposed a qualitative model based on the charge state of the lower SOIinterface to explain the dependence of the anomalous effect on substrate bias. The model for current-voltage characteristics in subthreshold region for sub micrometer fully- depleted SOI-MOSFET. The above slope is computed for I_D vs V_G curve in subthreshold region with V_{DS} kept asconstant.

Fossum, et al. [12] the model for current-voltage characteristics in subthreshold region for submicrometer fully-depleted SOI-MOSFET was proposed. Observed the abnormally large drain current in subthreshold region and related it to the floating body effects due to the impact-ionization at the drain. The analytical model for subthreshold current voltage characteristics taking into account the dependence of effective depletion charge on the drain bias and the voltage drop in the substrate region underneath the buried oxide. Short channel effects like threshold voltage roll off and drain induced barrier lowering were also analyzed for a gatelength up to 0.25 μm.

Woo et al. [13] separated the 2D Poisson's equation into a one-dimensional Poisson's equation and 2D Lapalace equation. To solve the 2D Poisson's equation Green's function technique can also be applied as demonstrated for a bulk MOSFET and for a short channel length MOSFET. The exact solution of the 2D Poisson's equation for the fully depleted SOI MOSFET has been derived using three zone Greens function technique. Also a symmetric dual-material dual-gate MOSFET structure has been analyzed. A 2D analytical model was developed for potential and electric field distribution in the body region and the threshold voltage assuming uniform distribution in the body region. Asymmetric double material fully depleted silicon on insulator MOSFET has also been analyzed assuming uniform distribution in the body region.

Asymmetrical double-gate (DG) CMOS, utilizing n+ and p+ polysilicon gates, can be superior to symmetrical-gate counterparts. The most noteworthy result was that asymmetrical DG MOSFETs, optimally designed with only one predominant channel, yield comparable, and even higher drive currents at low supply voltages. An explicit analytic solution of the surface potential of undoped-body symmetric dual-gate devices. The error produced by the proposed solution compared to exact results is reasonably small for typical device dimensions and bias conditions.

CHAPTER 3

POTENTIAL AND ELECTRIC-FIELD DISTRIBUTION IN DM DG MOSFET

3.1 Introduction

According to the Brew's scaling theory [14], the doping concentration in the body should be increased in the bulk *Si MOSFET* to alleviate the short-channel effects. Typically, the required doping concentration for a gate length less than *0.1* μ*m* is more than 10^{18} cm^{-3} [14]. Such high-doping concentration degrades device performance due to decreased mobility and increased junction capacitance. A DG FD SOI-MOSFET (figure 3.1), was proposed to overcome the scaling limitations of bulk *Si MOSFETs*. In this structure two gates simultaneously control the carrier charge and current flow through the body region [15].

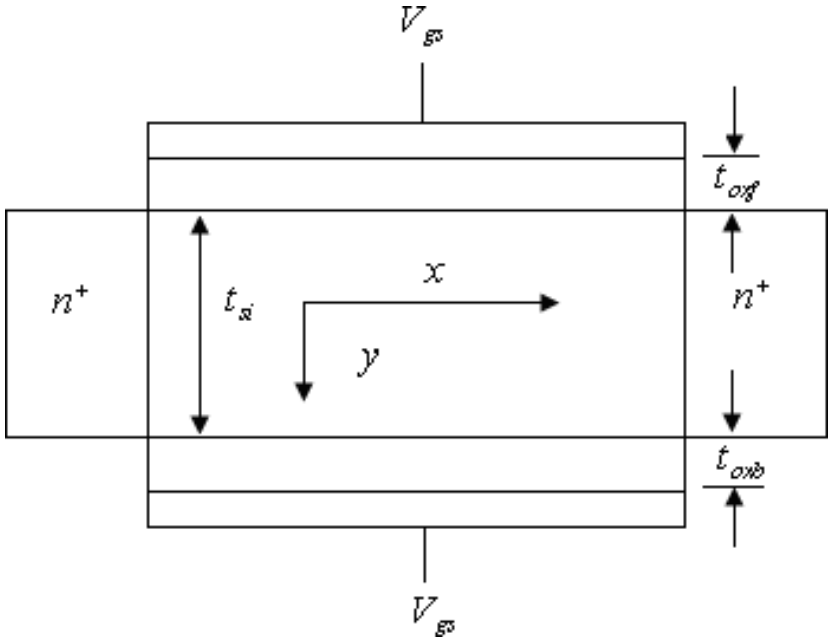


Figure 3.1: Cross-sectional view of a Double-Gate Fully-Depleted SOI MOSFET

Excellent high speed and performance have been achieved in *DG FD SOI MOSFET* through improved design, use of high quality material and processing innovations [15]. It may be mentioned that in bulk Si MOSFET, the threshold voltage decreases as

the channel length shrinks, due to charge sharing between the source and drain. This problem is effectively solved in DG FD SOI MOSFETs due to a small channel depth [16].

The potential distribution in DG FD SOI MOSFET differs greatly from that in bulk Si MOSFET because in the former the device structure is symmetric and body doping concentration is low [17]. In double-gate SOI MOSFETs, the potential in the middle of the channel is more sensitive to the gate length than that at the surface. The whole silicon film is into strong inversion in case of DG FD SOI MOSFETs. As the entiresilicon layer is able to carry the current, the current capability of these devices is greater than that of bulk Si MOSFETs.

It has been demonstrated that the DG FD SOI MOSFET structure offers greatly reduced short channel effects but does not improve the electron transport efficiency. Electron transport efficiency (assuming n-channel MOSFET) is related to the average electron transport velocity traveling through the channel which depends on the electric field distribution along the channel. In a MOSFET, in general, electrons enter into the channel initially with a low velocity and gradually get accelerated towards the drain. The electrons move fast in the region near drain but comparatively slow in the region near the source. Therefore, the performance of the device is affected by the relatively low electrondrift velocity in the channel near the source.

In this work, a structure named as symmetric DM DG FD SOI MOSFET which offers improved electron transport efficiency, is proposed. The proposed structure, as shown in the figure 3.2, has two metals in the gate (both side) M_1 and M_2 with different work functions. The work function of metal gate M_1 is greater than the work function of metal gate M_2 for n-channel MOSFET and vice-versa for a p-channel MOSFET. Due to this work function difference, the gate transport efficiency is improved by modifying the electric field distribution and surface potential profile. The step potential profile ensures reduction in SCEs. Also the peak electric field at the drain side isreduced, which ensures that the average electric field under the gate is increased leading to greater control of gate over the conductance of the channel which in turn leads to the increased electron transport efficiency. The overall device performance (particularly RF performance) greatly depends upon the doping distribution in the body region.

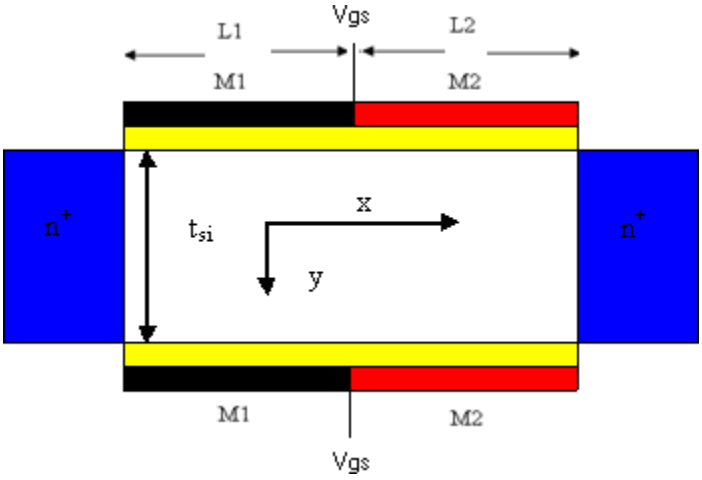


Fig 3.2 Cross-sectional view of a symmetric Dual-Material Double-Gate Fully-Depleted SOI MOSFET

For the purpose of *IC* design the near exact device model is essential. Therefore, it is necessary to carry out the analysis for exact relationship between the device material and structure parameters with the electrical characteristics of the device. For this, the device behavior needs to be analyzed assuming a doping distribution as close to practically obtained doping distribution as possible. For improved device performance, the bodyregion is doped by ion implantation process.

3.2 Ion Implantation in Thin Silicon Film

The introduction of ions into a substrate for changing its properties is called ion-implantation. During ion implantation, dopant atoms are vaporized, accelerated and directed at a silicon substrate.

The beam of ionized dopants enters the crystal lattice, collide with silicon atoms, and gradually lose energy, finally coming to rest at some depth within the lattice. The average depth is controlled by adjusting the energy and dose of the dopant. For the dopant, ion energies varying from 1 keV to 1 MeV, the average penetration depth varies from 100 Å to 10 µm. The range of ion dose varies from 10^{12} ions/cm^2 for threshold adjustment to 10^{18}

ions/cm^2 for buried insulators. Ion implantation is used to replace the chemical or doped oxide source wherever possible and is extensively used in device fabrication.

3.3 Doping Distributions

As discussed, the performance of the device depends greatly on impurity profile, in the body region. The implanted ion distribution in general is given by

$$N_a(y) = N_d \, . \, f(y) \qquad (3.1)$$

Where Nd is the total implant dose per unit area and *f(y)* is the probability density function (*PDF*).

The parameters associated with this *PDF*, $f(y)$, are given by

The projected range, $R_p = \int_{-\infty}^{\infty} y.f(y)dy$ (3.2)

The standard deviation $\sigma = [\int_{-\infty}^{\infty}(y - R_p)^2.f(y)dy]^{1/2}$ (3.3)

The skewness $\gamma = \int_{-\infty}^{\infty}(y - R_p)^3.f(y)dy/\sigma^3$ (3.4)

Kurtosis is a measure of the combined weight of a distribution's tails relative to the center of the distribution. When a set of approximately normal data is graphed via a histogram, it shows a bell peak and most data within three standard deviations (plus or minus) of the mean.

The kurtosis $\beta = \int_{-\infty}^{\infty}(y - R_p)^4.f(y)dy/\sigma^4$ (3.5)

These parameters are determined so as to fit an assumed function to an experimentally determine doping profiles [18-20], with the condition, = $\int_{-\infty}^{\infty} f(y)dy = 1$. The numerical values for these parameters are given in papers [21,22] and fitted to a polynomial in paper [23] through for $R_p = \sum_{i=1}^{n} a_i \, . \, E^i$ (3.6) $and\ \sigma = \sum_{i=1}^{n} b_i \, . \, E^i$ (3.7) for n = 1,2,3,4…… Here, *E* is the implantation energy and *a* & *b* are the coefficients for silicon as target.

3.4 Uniform Distribution

The Uniform distribution is a special case of equation (3.1) with $f(y) = 1$.

Gaussian Distribution

This is the simplest approximation to an Ion-implanted Profile. This profile is characterized by the projected range (Rp), the average depth of the implanted ions and standard deviation (σ) the distribution of ions about that depth. The probability density function f(y) for a Gaussian distribution is given as

$$f(y) = \frac{1}{\sqrt{2\pi}} . Exp(-\frac{(y-R_p)^2}{2.\sigma^2} \qquad (3.6)$$

Gaussian distributions have a skewness of "zero" and a kurtosis of "three". The approximation of implanted doping profile with a Gaussian distribution is only

accurate up to first order. The Gaussian distribution with different (Rp) and different standard deviation (σ) is shown in figure 3.3 (a) and (b) respectively.

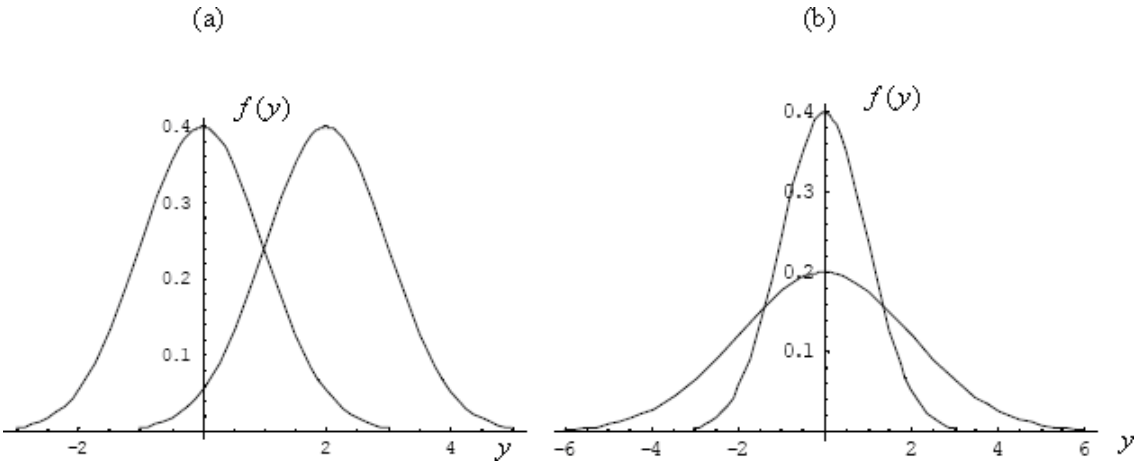


Figure 3.3: Gaussian distribution with different (a) means and (b) standard deviations

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3.5 Dual-Material Double-Gate MOSFET Operations

In dual-material double-gate *SOI MOSFET*, the front gate and the back gate consists of dual materials of different work functions as shown in figure 3.2. In general, the front gate bias voltages are chosen to be different to achieve optimal performance of the device.

The relationship between the two gate voltages is: $V_{gs1} = K V_{gs2}$, where the coefficient K accounts for the difference in the two gate in respect of the threshold voltages. In our calculation K =1 is considered so that both the gates are at the same potential. The thickness of the *Si* layer has been assumed to be less than x_{dmax}, where

$$x_{dmax} = \sqrt{\frac{4.\varepsilon_{Si}}{q.N_a(y)_{max}}}.\varphi_F \qquad (3.7)$$

Here x_{dmax} is the maximum depletion width and $N_a(y)$ max is the maximum dopant concentration in Si. This ensures that the Si body is fully depleted.

3.5.1 Potential Distribution

Potential distribution is an important parameter in device modeling, [14] as many other parameters are determined from it i.e. threshold voltage, channel field etc.

Assuming,

$$\frac{\partial^2\varphi(x,y)}{\partial_{x^2}} + \frac{\partial^2\varphi(x,y)}{\partial_{y^2}} = \frac{q.N_a(y)}{\varepsilon_{Si}} \qquad (3.8)$$

for 0 £ x £ L_g and 0 £ y £ t_{si}, where, $N_a(y)$ is the doping distribution, dependent on the thickness of the silicon layer. q is the electron charge, ε_{si} is the permittivity of the silicon, L_g (L_1 + L_2) is the gate length and t_{si} is the silicon layer thickness.

The method for finding the analytical solution for f (x, y) involves simplify the two dimensional Poisson's equation into a one-dimensional equation with the help of appropriate conditions. At low drain-source voltage the x -dependence of potential f (x, y) for fully depleted SOI MOSFET can be approximated by a simple parabolic function [16].

$$\Phi(x,y) = A_0(x) + A_1(x).\, y + A_2(x).y^2 \qquad (3.9)$$

where, $A_0(x)$, $A_1(x)$, $A_2(x)$ are functions of x only. Equation (3.9) requires three conditions to have a non-trivial solution. In Dual-Material Double-Gate structure, we have two different materials in both the gates (front as well as back) with work functions φ_{M1} and φ_{M2}, respectively. The potential distribution under gate M_1, $\varphi_1(x, y)$ and under gate M_2, $\varphi_2(x, y)$ respectively can be written as are arbitrary coefficients.

$$\Phi_1(x,y) = A_{10}(x) + A_{11}(x).\, y + A_{12}(x).y^2 \qquad \text{for } 0 \le x \le L_1 \text{ and } 0 \le y \le t_s \qquad (3.10)$$

$$\Phi_2(x,y) = A_{20}(x) + A_{21}(x).\, y + A_{22}(x).y^2 \qquad \text{for } L_1 \le x \le L_1 + L_2 \text{ and } 0 \le y \le t_{si} \qquad (3.10)$$

Where $A_{10}(x)$, $A_{11}(x)$, $A_{12}(x)$, $A_{20}(x)$, $A_{21}(x)$ and $A_{22}(x)$ are arbitrary coefficients.

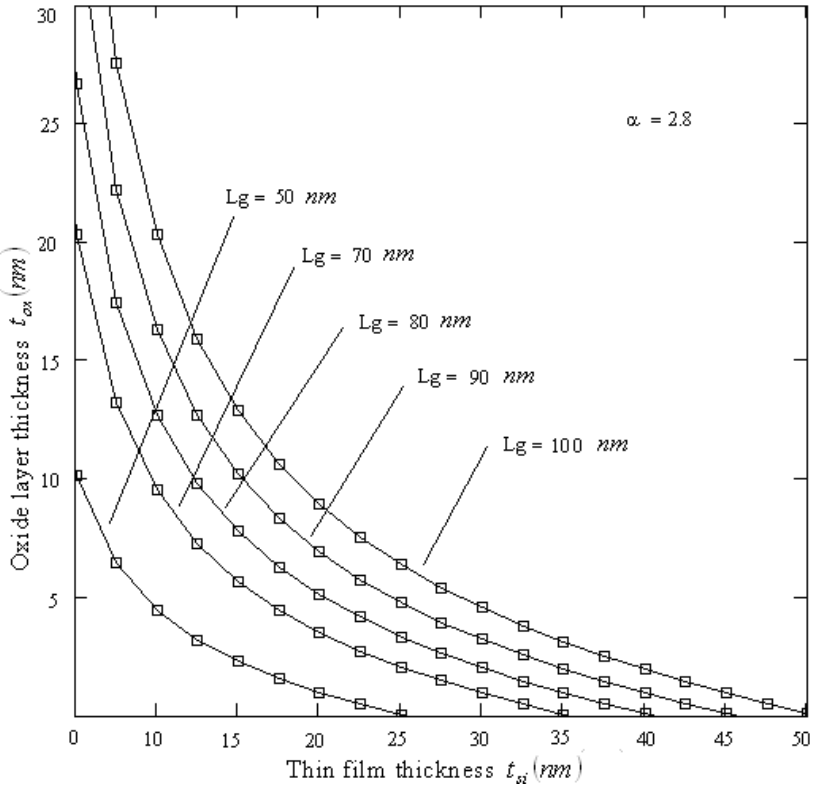

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Figure 3.4: Relationship between oxide layer thickness, *ox t* and silicon layer thickness, *si t* for different values of gate length

3.5.2 Surface Potential

In figure 3.5, ϕ_s and ϕ_c for both DM DG and SM DG SOI MOSFET is plotted. For SM DG SOI MOSFET, the metal work function is assumed to be V ϕ_M =5. It is evident that the absolute value of ϕ_c is smaller than the ϕ_s [15]. It is also observed that the potential at the surface and center exhibits a step function in the surface. Due to this step function, the area under M_1 of front gate of the DM DG structure is screened from the drain potential variations or we can say the step function suppresses the effect of the electric field induced by the drain-source potential in the region under M_1.

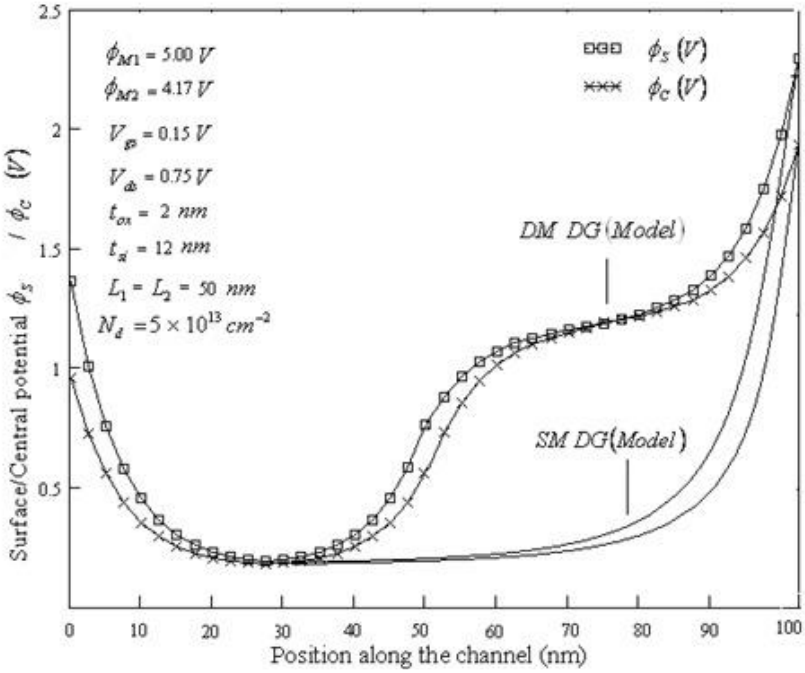

Figure 3.5: Potential profile at the surface and center of DM DG and SM DG FD SOI MOSFET (Model) for a channel length Lg = 100nm

This means that the drain potential has very little effect on the drain current after saturation increasing the drain resistance. Figure 2.10 shows the comparison between the values calculated using analytical model and the corresponding values obtained using numerical solution (using *ATLAS*) for *DM DG* structure. As is evident from the figure 2.10, the calculated results using the analytical model are in excellent agreement with the simulation results (obtained using *ATLAS*).

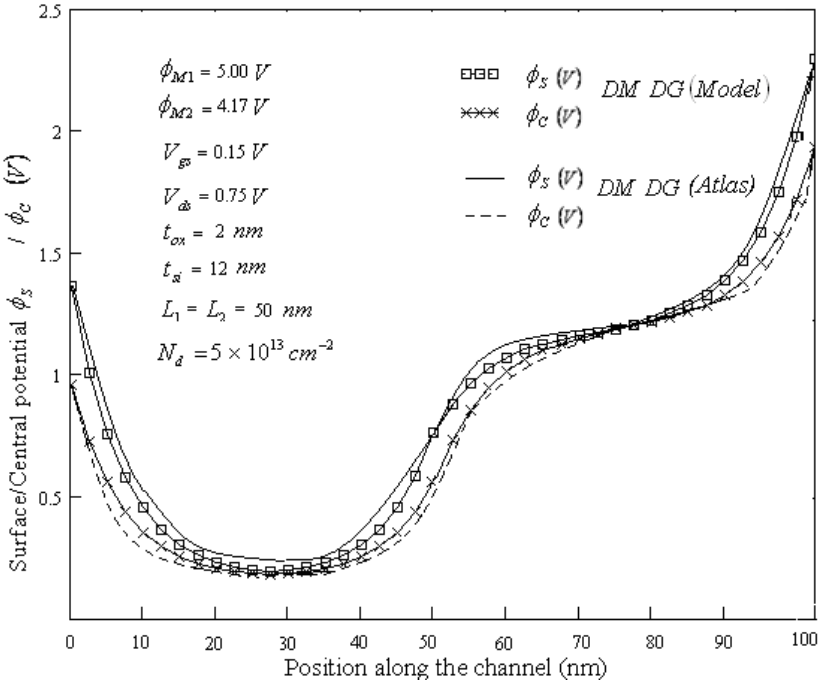

Figure 3.6: Comparison of analytical model and simulated values of potential at the Surface and center of DM DG FD SOI MOSFET for a channel length Lg = 100nm

Figure 3.7 shows the surface potential variation along the channel for t_{si} = 6 nm keeping other parameters as such. It is observed that the difference between the surface and center potential decreases as we decrease the film thickness, because for small silicon layer thickness, the center potential approaches towards surface potential. This means there is no significant difference between the two potentials when the film thickness is very small. Step function of potential becomes more flat as we decrease the silicon layer thickness as shown in figure 3.8. This is due to one-dimensional nature of electric field over major part of the device.

Figure 3.9 shows the variation of surface potential in DM DG FD SOI MOSFET for long channel length Lg = 1000 nm . It is observed that the constant potential contour in a long channel device is mostly parallel to the 2 Si / SiO interface thereby making electric field one dimensional over most part of the device. The surface potential as calculated using the analytical model and as obtained using device simulator ATLAS is also compared in figure 3.9. As can be seen, the two results in excellent agreement.

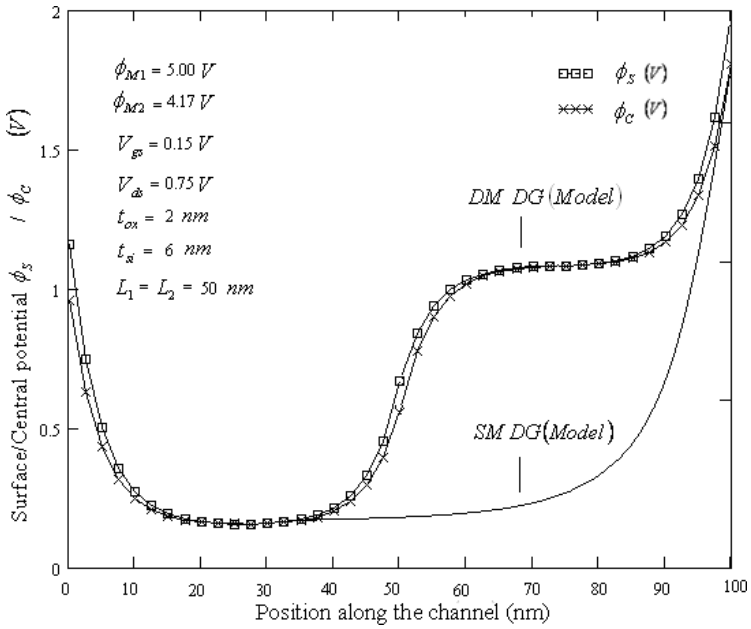

Figure 3.7: Potential profile at the surface and center of DM DG and SM DG FD SOI MOSFET (Model) for a channel length L_g = 100nm and t_{si} = 6nm

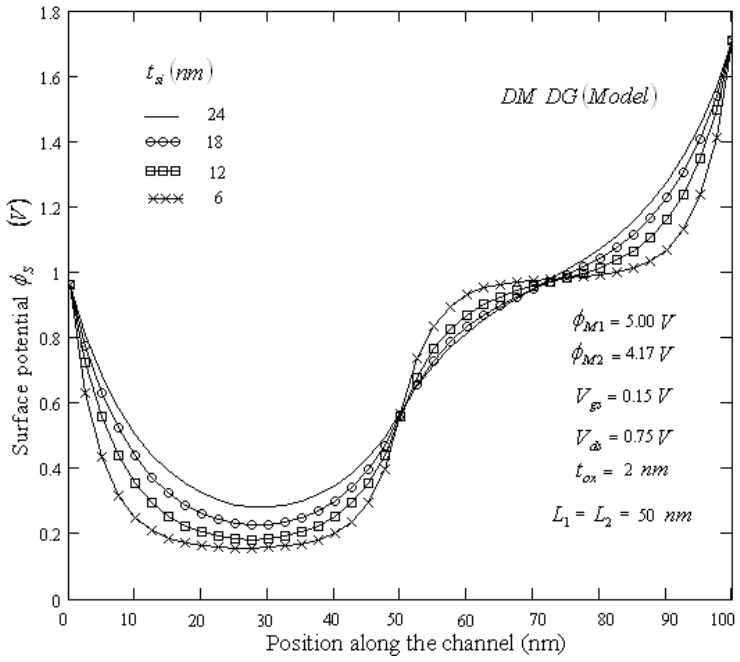

Figure 3.8: Potential profile at the surface of DM DG FD SOI MOSFET (Model) for a channel length L_g = 100nm for different values of film thickness

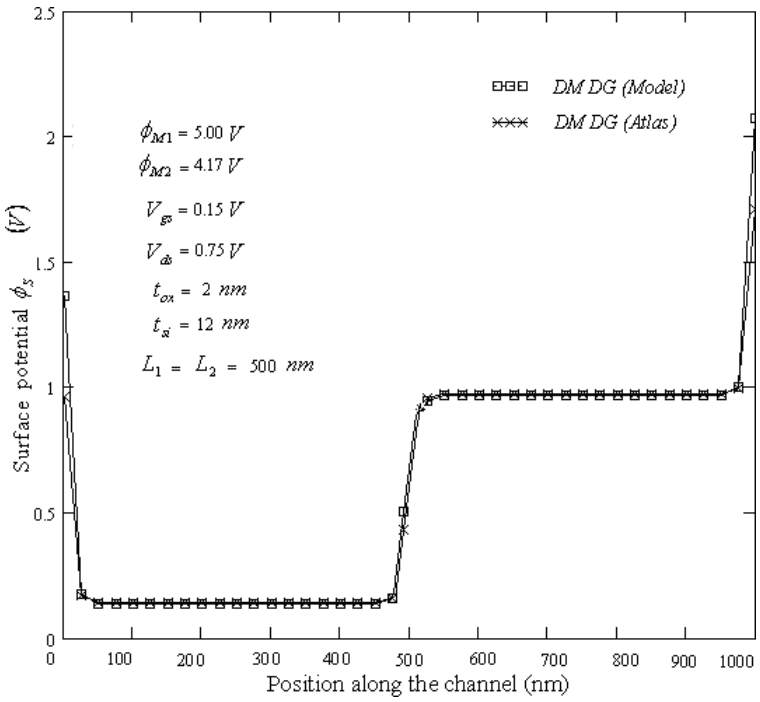

Figure 3.9: Potential profile at the surface of DM DG FD SOI MOSFET (Model) for a channel length L_g = 1000nm

On comparing figure 3.9 and figure 3.8, where L_g =100 nm, it is seen that the constant potential contour becomes more curvilinear as the gate length decreases. This curvilinear nature of potential is due to the two-dimensional nature of the electric field in the channel. Figure 3.10 shows the variation of the surface potential along the channel length for different values of oxide thickness for *DM DG* structure. On increasing the value of oxide thickness t_{ox} at the front end as well as at the back end , M_1 and M_2 lose their control. over the channel thereby increasing the DIBL. However, continuous decrease in the oxide thickness definitely reduces the DIBL, but at the same time we have to account the tunneling across the thin oxide and hot-carriers effects. surface potential for higher values of V_{ds}. Hence, the area under M1 is screened from the changes in the V_{ds} . However, there

is enhancement in the values of surface potential near drain for increasing values of V_{ds} as shown in the figure 3.11.

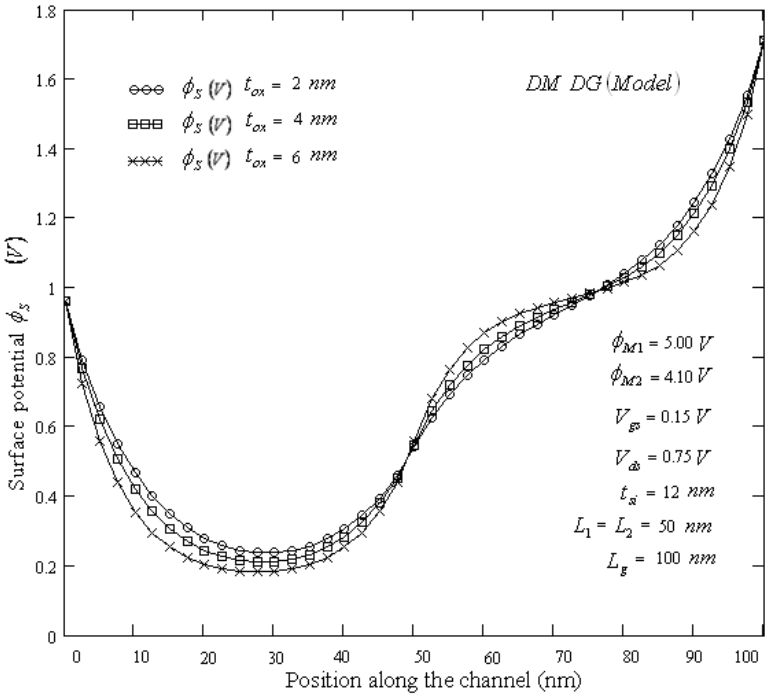

Figure 3.10: Potential profile at the surface of DM DG FD SOI MOSFET (Model) for a channel length L_g = 100nm for different values of oxide thickness

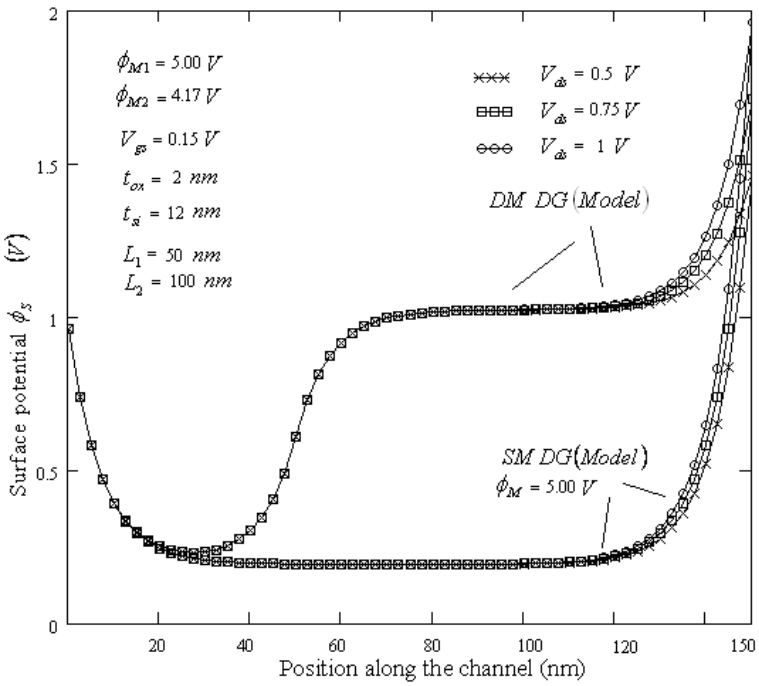

Figure 3.11: Potential profile at the surface of DM DG FD SOI MOSFET (Model) for a channel length L_g = 150nm where $L_1 \neq L_2$, for different values of V_{ds}

CHAPTER 4

SIMULATION RESULTS AND DISCUSSION

4.1 Results and Discussion

In this chapter, the analytical expressions for the various device parameters (relevant to the switching behaviour of the *MOSFET*) have been derived for the basic physical consideration using approximate boundary conditions. The parameters are Threshold voltage, Device capacitance, drain current, Transconductance, Drain resistance and Cut-off frequency. Noise can also be considered. Detail analysis of above parameter have been carried out in this chapter with reference to double gate metal oxide semiconductor field effect transistor.

4.1.1 Threshold Voltage

The threshold voltage can be defined as gate voltage for which the minimum surface potential is twice the Fermi potential. Since the same metals are used on both the gates, the threshold voltages on both the gates are equal. Substituting $\varphi_{s1}(x_{min}, t_{si}/2)=2.\varphi_F$ and $V_{gs} = V_{th}$), the threshold voltage obtained is given as

$$V_{th} = \frac{-G7 + \sqrt{G7^2 - 4.G6.G8}}{2.G6} \tag{4.1}$$

The derivation of the above equation and the expressions of G_6, G_7 and G_8 are given. In *DM DG SOI* structure, the position of x_{min} lies under the metal gate M_1 (both side) because $V_{FB1} > V_{FB2}$ and therefore, the effective gate voltage under the M_1 region is less than that for M_2. Figure 4.1 shows the variation of threshold voltage of *DM DG* and *SM DG* structure along the channel length under L_2 for fixed value of $L_1 = 50$ *nm*. It is observed that the threshold voltage rolls up in case of *DM DG SOI* structure in comparison to the rolls down for *SM DG SOI* structure with decreasing channel length. It is because of increasing L_1/L_2 ratio and increasing portion of the larger work function 100 gate as the channel length reduces. This is a unique feature which gives *DM DG* structure an added advantage when the device dimensions are continuously shrinking. It can also be seen in figure 4.2 that the threshold voltage as calculated using analytical equation 4.1 is in close agreement with the same computed using device simulator *ATLAS*.

Except this roll up, the threshold voltage of the *DM DG* structure is about the same as a *SM DG* structure having the same gate material as M1 of the *DM DG* structure.

Therefore, the channel region under M_2 has more freedom of optimization. For instance, the substrate doping of this region can be reduced, thereby it has added advantage that source and drain capacitance can be decreased, while potentially improving the speed over the conventional device.

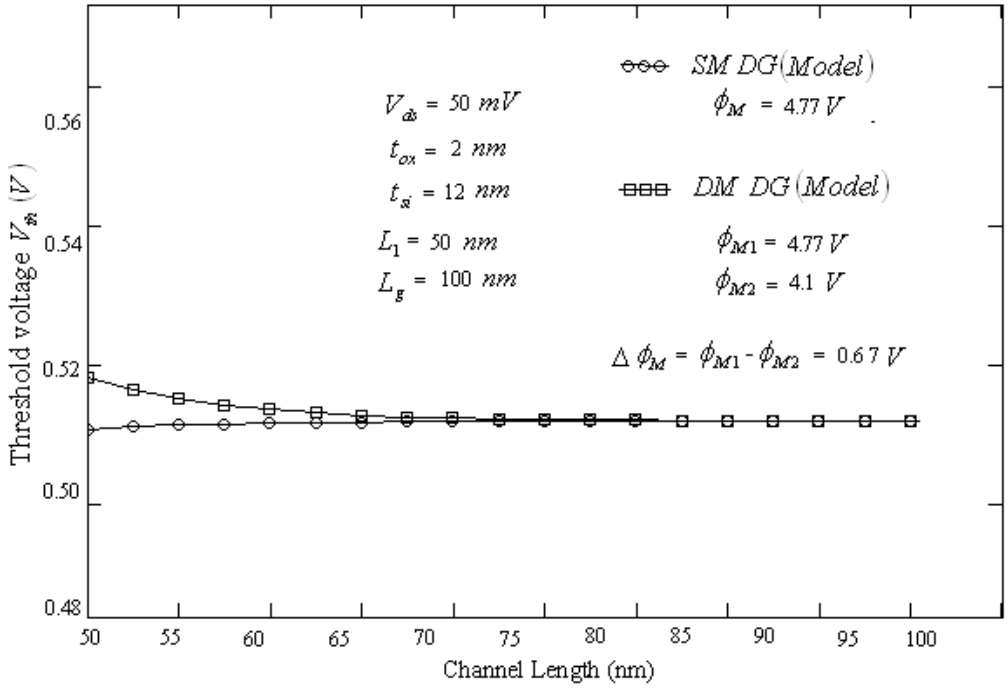

Figure 4.1 Threshold voltage along the channel for fixed L_1 = 50 nm in SM DG and DM DG structures

When the difference between the work function of M_1 and M_2 changes, the threshold voltage also changes, as shown in figure 4.3. From figure 4.2 and figure 4.3, it is evident that if the work function difference increases the threshold voltage also increases, as predicted by equation (4.1). When the device is on then the screen gate shields the region under the control gate from any drain voltage variations and in this way, screen gate absorbs any additional drain to source voltage beyond saturation. This in turns leads to reduction in DIBL.

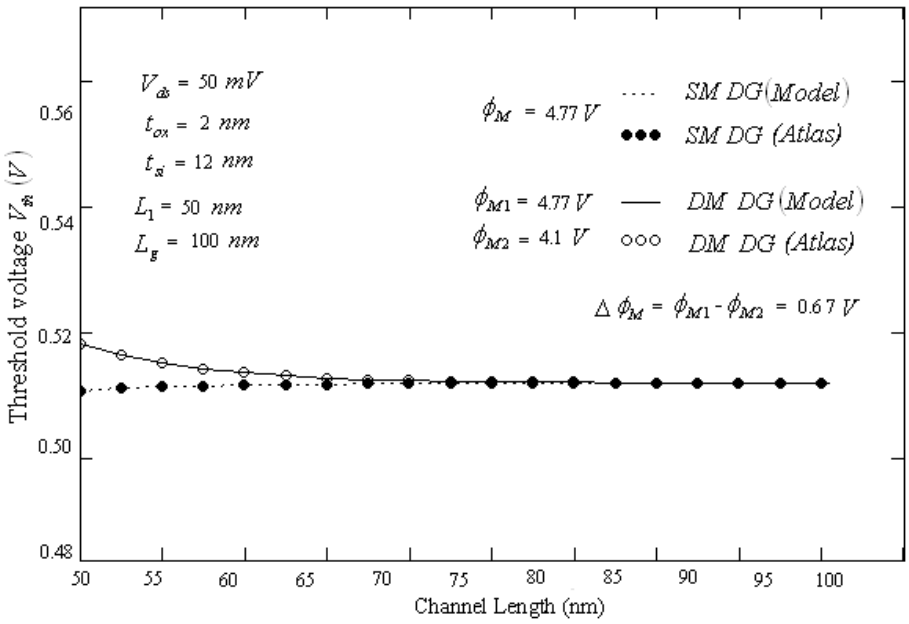

Figure 4.2 Comparison of analytical model with simulated values of threshold voltage for fixed L_1 = 50 nm in SM DG and DM DG structures

Table 4.1: Threshold voltage along the channel in DM DG structure for different doping distribution

Position along the Channel (nm)	Threshold Voltage (V)	Threshold Voltage (V)	Threshold Voltage (V)
DM DG Model	Pearson	Gussian	Uniform
50	0.26	0.28	0.31
55	0.26	0.28	0.31
60	0.26	0.28	0.31
65	0.26	0.28	0.31
70	0.26	0.28	0.31
75	0.26	0.28	0.31
80	0.26	0.28	0.31
85	0.26	0.28	0.31
90	0.26	0.28	0.31
95	0.26	0.28	0.31
100	0.26	0.28	0.31

V_{ds} = 50 mV, φ_{M1} =4.44 V, t_{ox} = 2 nm, φ_{M2} =4.1 V

t_{si} = 12nm, L_1 =50 nm, L_g =100 nm

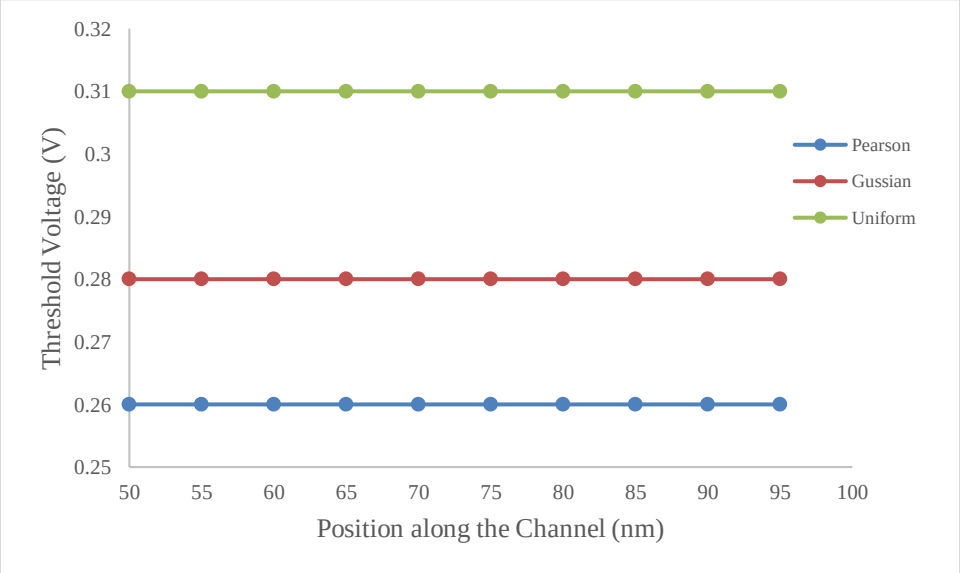

Figure 4.3 Threshold voltage along the channel in DM DG structure for different doping distribution

4.1.2 Device Capacitance

The equivalent circuit of *DM DG FD SOI MOSFET*, ignoring the resistance, is shown in figure 4.4 (a). Here *CGS = CSG = CGD = CDG* as the device is symmetric.

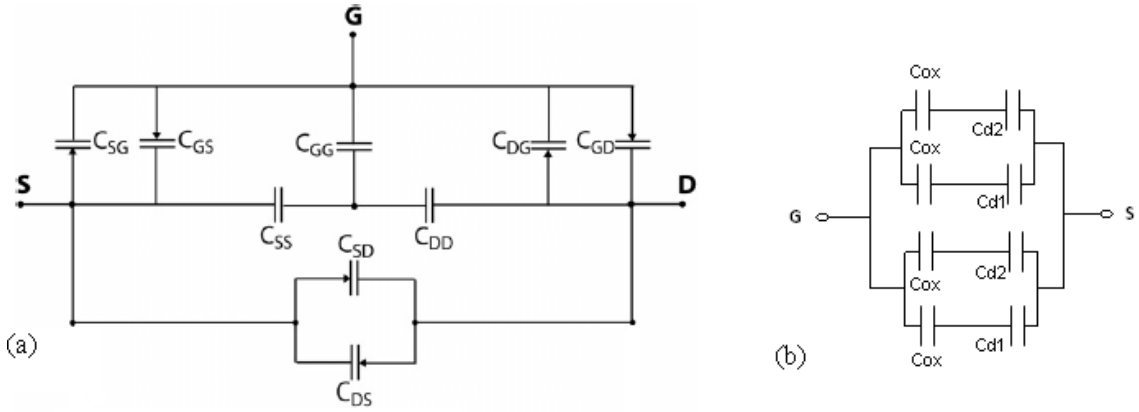

Figure 4.4 (a) Equivalent circuit of DM DG FD SOI MOSFET (b) Simplified circuit for C_{GS}

In figure 4.4, *CGS* is gate-source trans capacitance, similarly, *CGD*, *CSG* and *CDG* are gate drain, source-gate and drain-gate capacitance. *CSS* and *CDD* are source and drain self capacitances. In a *DG SOI MOSFET*, the depletion regions charge under M_1 and M_2 [40, 41] are given by

$$Q_{d1} = \sqrt{2.q.N_a\left(\frac{t_{si}}{2}\right).\varepsilon_{si}}.\sqrt{\phi_{s1}(x)} \quad \text{for} \quad 0 \le x \le L_1 \tag{4.2}$$

$$Q_{d2} = \sqrt{2.q.N_a\left(\frac{t_{si}}{2}\right).\varepsilon_{si}}.\sqrt{\phi_{s2}(x)} \quad \text{for} \quad L_1 \le x \le L_1 + L_2 \tag{4.3}$$

Here $N_a(t_{si}/2)$ N is the doping concentration, calculated at y= $t_{si}/2$. The different capacitances associated are obtained as follows:

(a) The depletion layer capacitance is the rate of change of depletion layer charge with gate voltage and is given by

$$C_{d1} = \frac{dQ_{d1}}{dV_{gs}} = \sqrt{\frac{q.N_a\left(\frac{t_{si}}{2}\right).\varepsilon_{si}}{2.\phi_{s1}(x)}}.\frac{d\phi_{s1}(x)}{dV_{gs}} \qquad (4.4)$$

$$C_{d2} = \frac{dQ_{d2}}{dV_{gs}} = \sqrt{\frac{q.N_a\left(\frac{t_{si}}{2}\right).\varepsilon_{si}}{2.\phi_{s2}(x)}}.\frac{d\phi_{s2}(x)}{dV_{gs}} \qquad (4.5)$$

Where

$$\frac{d\phi_{s1}(x)}{dV_{gs}} = 1+\frac{E_2-E_3}{E_1}.\exp\left(\frac{x}{\lambda_1}\right)+\frac{E_3-E_5}{E_1}.\exp\left(-\frac{x}{\lambda_1}\right) \quad \text{for} \quad 0 \le x \le L_1$$

$$\frac{d\phi_{s2}(x)}{dV_{gs}} = 1+\frac{(C_1+C_2)}{C_5}.\exp\left(\frac{x-L_1}{\lambda_1}\right)+\frac{C_3+C_4}{C_5}.\exp\left(-\frac{(x-L_1)}{\lambda_1}\right)\exp\left(\frac{L_2}{\lambda_1}\right)$$

$$\text{for } L_1 \le x \le L_1+L_2$$

$$E_1 = \exp\left(\frac{L_g+L_2}{\lambda_1}\right)-\exp\left(\frac{-L_g+L_2}{\lambda_1}\right); \qquad E_2 = \exp\left(\frac{-L_g+L_2}{\lambda}\right);$$

$$E_3 = \exp\left(\frac{L_g-L_1}{\lambda}\right); \qquad E_5 = \exp\left(\frac{L_g+L_2}{\lambda}\right)$$

$$C_1 = -1+\exp\left(\frac{2.L_2}{\lambda_1}\right); \qquad C_2 = \exp\left(\frac{L_1+L_2}{\lambda_1}\right)-\exp\left(\frac{L_1+3.L_2}{\lambda_1}\right)$$

$$C_3 = -\exp\left(-\frac{L_1}{\lambda_1}\right)+\exp\left(-\frac{L_1-2.L_2}{\lambda_1}\right); \qquad C_4 = \exp\left(\frac{L_2}{\lambda_1}\right)-\exp\left(\frac{3.L_2}{\lambda_1}\right);$$

$$C_5 = \left(\exp\left(\frac{L_1+2L_2}{\lambda_1}\right)-\exp\left(-\frac{L_1}{\lambda_1}\right)\right)\left(-1+\exp\left(\frac{2L_2}{\lambda_1}\right)\right)$$

$$C_{GS} = 2.\frac{(C_{d2}.C_{ox}).(C_{d1}+C_{ox})+(C_{d1}.C_{ox}).(C_{d2}+C_{ox})+C_{ss1}.(C_{d2}+C_{ox}).(C_{d1}+C_{ox})}{(C_{d2}+C_{ox}).(C_{d1}+C_{ox})} \quad (4.6)$$

Where $C_{GS} = C_{SG} = C_{GD} = C_{DG}$

The interface capacitance, C_{ss1} is given by $C_{ss1} = q.N_{ss}$, where N_{ss} $(cm^{-1}\ eV^{-1})$ is the interface state density.

The depletion layer capacitance of *DM DG FD SOI MOSFET* as a function of gate to source voltage for surface potential is shown. Correspondingly, the device depletion capacitance is plotted as a function of gate to source voltage in *SM DG FD SOI MOSFET* also, using the analytical model. It is seen that the depletion capacitance is much larger in case *SM DG* structure particularly for a small value of gate to source voltage. This is expected because in *SM DG* structure the metal chosen had larger work function. In figure 4.5, the calculated value of the gate-source capacitance vs gate to source voltages as obtained using analytical model for *SM DG* and *DM DG* structures.

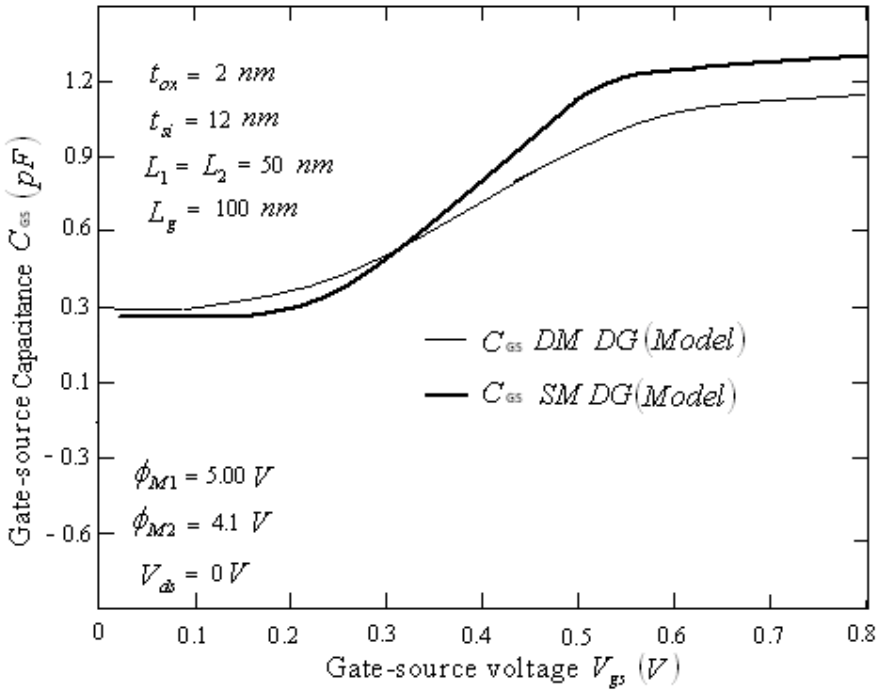

Figure 4.5: Gate-to-source capacitance vs gate-source voltage for DM DG and SM DG structures

Table 4.2: Depletion Layer Capacitance Vs Gate-Source Voltage Based on Surface Potential

S.No.	Gate-Source Voltage V_{gs} (V)	Depletion Capacitance C_d (pF)
1.	0.0	0.25
2.	0.2	0.22
3.	0.3	0.20
4.	0.4	0.18
5.	0.6	0.16
6.	0.7	0.15
7.	0.9	0.14
8.	1.0	0.13
9.	1.2	0.12
10.	1.3	0.12

t_{ox} = 2 nm, t_{si} = 12nm, L_1= L2 =50 nm, L_g =100 nm, φ_{M1}=5.00 V, φ_{M2} =4.1 V, V_{ds} = 1 V

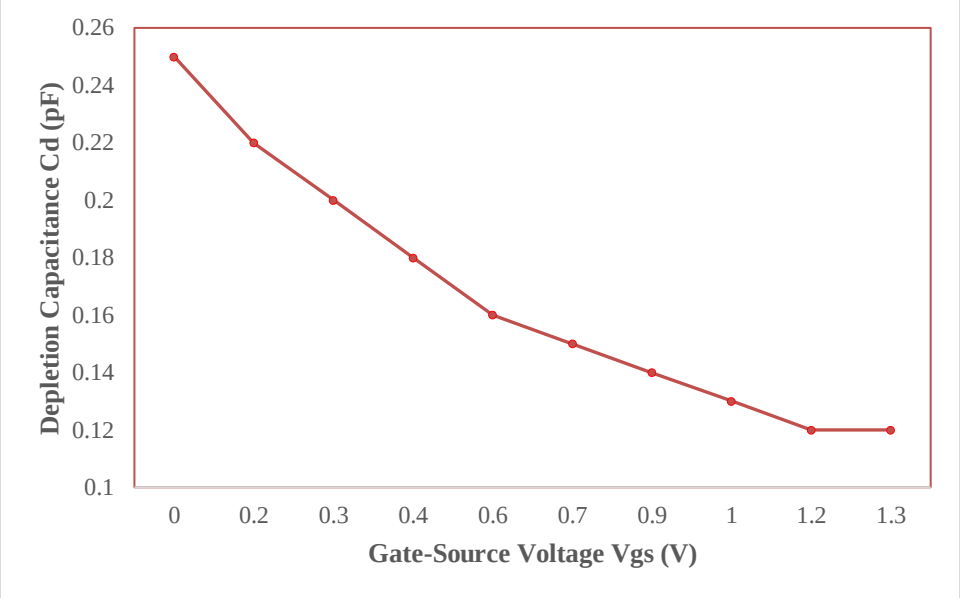

Figure 4.6: Depletion layer capacitance vs gate-source voltage based on surface potential

Figure 4.5 shows the C_{GS} is low in case of *DM DG* as compare to *SM DG* due to introduction of two metals in gate. The variation of the depletion capacitance with gate-to-source voltage for different doping distribution functions. It is seen that the depletion layer capacitance is low for devices having Pearson IV doping distribution.

The smaller value of depletion layer capacitance makes the device more useful for high speed as well as for the low power *VLSI* circuits. Because of the excess majority carriers accumulating under M_1 and M_2 of both sides of *DM DG FD SOI* structure, the depletion layer capacitances, C_{d1} and C_{d2}, due to V_{gs} -V_{fbf1} and V_{gs} -V_{fbf2}, becomes large. As the gate voltage further increases, the device capacitance decreases very fast.

The gate-to-source capacitance variation with respect to gate-to-source voltage for *DM DG FD SOI* structure. The results are shown to compare very well with simulations performed using the Silvaco Atlas device simulator.

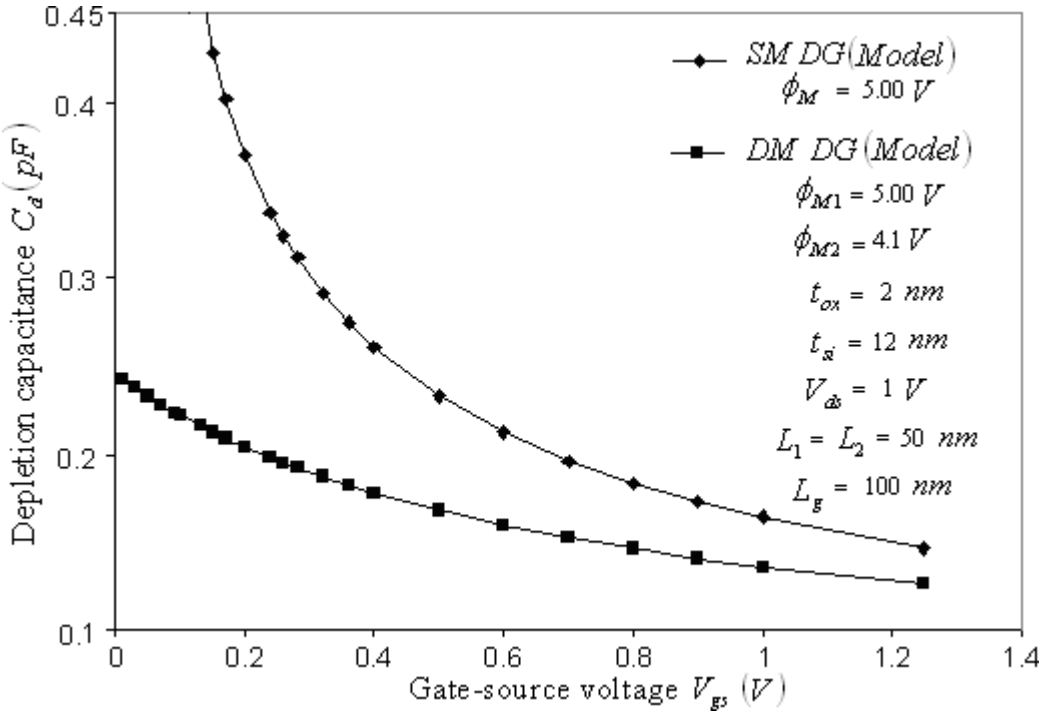

Figure 4.7: Depletion layer capacitance vs gate-to-source voltage in DM DG and SM DG structures

Table 4.3: Depletion layer capacitance in DM DG structure for different doping distribution

S.No.	Gate-Source Voltage V_{gs} (V)	Depletion Capacitance C_d (pF)		
		Pearson	**Gaussian**	**Uniform**
1.	0.0	0.25	0.31	0.38
2.	0.2	0.22	0.28	0.34
3.	0.3	0.20	0.25	0.30
4.	0.4	0.18	0.22	0.29
5.	0.6	0.16	0.19	0.27
6.	0.7	0.15	0.17	0.25
7.	0.9	0.14	0.16	0.24
8.	1.0	0.13	0.15	0.22
9.	1.2	0.12	0.15	0.21
10.	1.3	0.12	0.15	0.21

t_{ox} = 2 nm, , t_{si} = 12nm, L_1= L2 =50 nm, L_g =100 nm, φ_{M1} =5.00 V, φ_{M2} =4.1 V, V_{ds} = 1 V

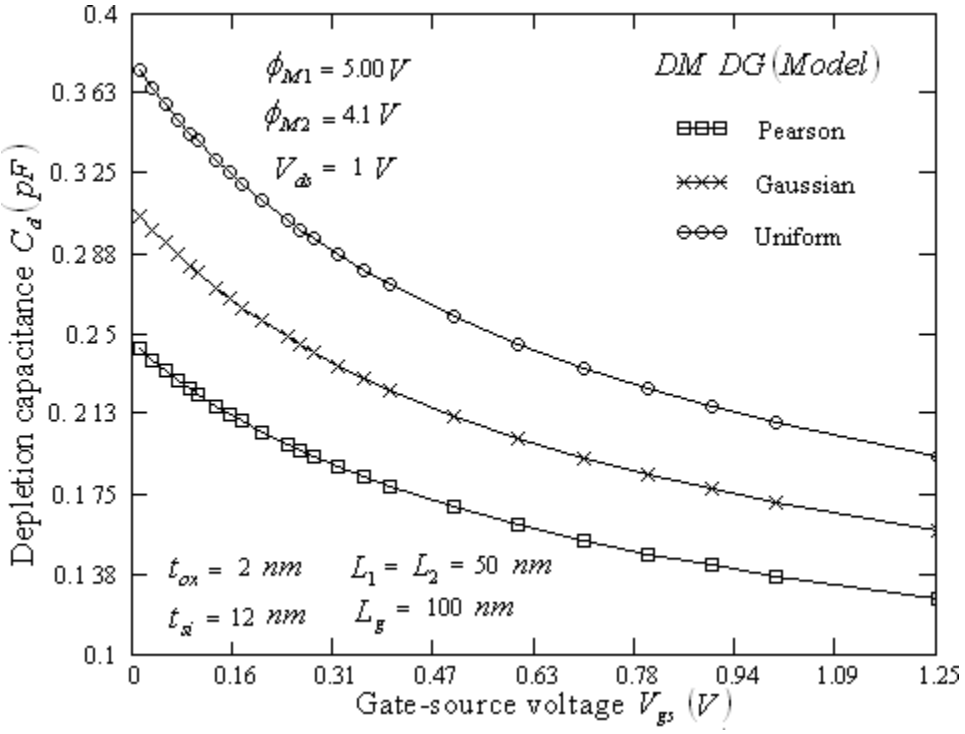

Figure 4.8: Depletion layer capacitance in DM DG structure for different doping distribution

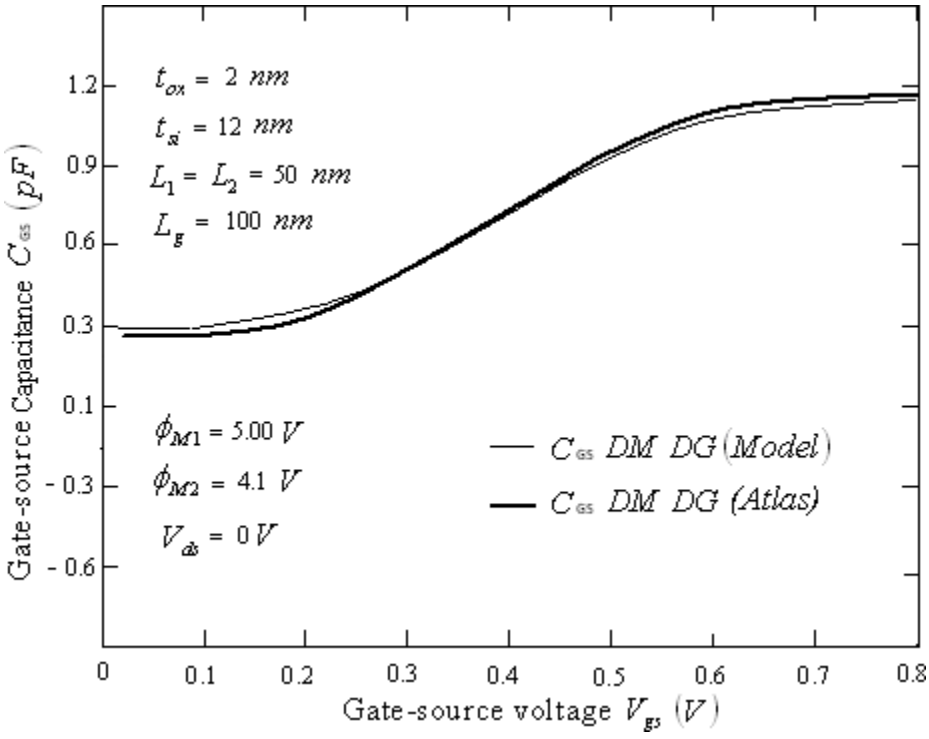

Figure 4.9: Gate-to-source capacitance in DM DG structure and its comparison with simulator's value

4..1.3 Drain-Current Characteristics

The current-voltage characteristics may be derived keeping in view the position dependent inversion layer charge and field dependent electron mobility. For a strongly inverted *n*-channel enhancement mode dual-material double-gate fully-depleted *SOI MOSFET*, the drain currents are given by

$$I_{ds} = -W.\mu_n(x).Q_n(x).\frac{d\phi_c(x)}{dx} \tag{4.7}$$

Where, $I_{ds} = I_1 + I_2$; $I_1 = -W.\mu_{n1}(x).Q_{n1}(x).\frac{d\phi_{c1}(x)}{dx}$, $I_2 = -W.\mu_{n2}(x).Q_{n2}(x).\frac{d\phi_{c2}(x)}{dx}$

I_{ds} is the drain current and W is the gate-width. As our device is symmetric, $Q_n(x)$, the inversion layer charge, is double of carrier charge under each gate

Here, Qs(x) and Qd are the surface charge and depletion layer charge densities. The surface charge is obtained using $Q_s(x) = -C_{ox}[V_{gs} + V_{sub} - V_{fbf} - \varphi_c(x)]$

Where, C_{ox}, is the oxide capacitance, V_{fbf} is the flat band voltage, V_{gs} is the applied gate-to-source voltage, $\varphi_c(x)$ is the potential at the center of the channel and V_{sub} is the substrate potential. The depletion layer charge is given by

$$Q_d = C_{ox}.[V_{fbf} - V_{th} + \phi_F] \tag{4.8}$$

Where V_{th} is the threshold voltage and φ_F is the Fermi potential. The field dependent mobility of electrons is given by

$$\mu_n(x) = \frac{\mu_{no}}{\sqrt{1 + \left(\frac{E(x)}{E_c}\right)^2}} \tag{4.9}$$

Where μ_{no} is the low field mobility, Ec is the critical field and E(x) is the lateral field given as

On substituting $Q_n(x)$ and $\mu_n(x)$ in equation (4.7), we get

$$I_{ds} = -W.\frac{\mu_{no}}{\sqrt{1 + \left(\frac{C_{ox}.(V_{fbf} - V_{gs} + \phi_c(x))}{\frac{\varepsilon_{si}}{E_c}}\right)^2}}.2.(-C_{ox}.(V_{gs} + V_{sub} + \phi_F - V_{th} - \phi_c(x)).\frac{d\phi_c(x)}{dx}$$

$$= \frac{2.W.\mu_{no}.C_{ox}}{\sqrt{1 + \left(\frac{C_{ox}}{\varepsilon_{si}.E_c}\right)^2 (V_{fbf} - V_{gs} + \phi_c(x))^2}}.(V_{gs} + V_{sub} + \phi_F - V_{th} - \phi_c(x)).\frac{d\phi_c(x)}{dx} \tag{4.10}$$

Integrating equation (4.10) using boundary conditions

$$E(x) = \frac{C_{ox}.(V_{fbf} - V_{gs} + \phi_c(x))}{\varepsilon_{si}}$$

$$\int_0^{L_1} I_1\,dx + \int_{L_1}^{L_g} I_2\,dx = \int_{V_{bi}}^{V_x} \frac{2.W.\mu_{no}.C_{ox}.(V_{gs} + V_{sub} + \phi_F - V_{th} - \phi_{c1}(x))}{\sqrt{1 + \left(\frac{C_{ox}}{\varepsilon_{si}.E_c}\right)^2 (V_{fbf1} - V_{gs} + \phi_{c1}(x))^2}}.d\phi_{c1}(x) +$$

$$\int_{V_x}^{V_{bi}+V_{ds}} \frac{2.W.\mu_{no}.C_{ox}.(V_{gs} + V_{sub} + \phi_F - V_{th} - \phi_{c2}(x))}{\sqrt{1 + \left(\frac{C_{ox}}{\varepsilon_{si}.E_c}\right)^2 (V_{fbf2} - V_{gs} + \phi_{c2}(x))^2}}.d\phi_{c2}(x)$$

$$= \int_0^{L_g} I_{ds}\,dx = I_{ds}.L_g$$

On solving for I_1 and I_2 separately, we get

$$I_{ds} = \frac{1}{L_g}\left[\left\{\frac{2.W.\mu_{no}.C_{ox}}{(d_3)^{\frac{3}{2}}} \times (1 + A_1) \times \left[(d_2 + d_4).\ln\left(\frac{c_1 + c_2}{c_{11} + c_{22}}\right) - c_2 + c_{22}\right]\right\} + \left\{\frac{2.W.\mu_{no}.C_{ox}}{(d_3)^{\frac{3}{2}}} \times (1 + A_1) \times \left[(d_2 + d'_4).\ln\left(\frac{c'_1 + c'_2}{c'_{11} + c'_{22}}\right) - c'_2 + c'_{22}\right]\right\}\right] \quad (4.11)$$

Where V*x* is calculated using

$$\int_{V_{bi}}^{V_x} I_{ds1}(L_1, 0)\,dx = \int_{V_x}^{V_{bi}+V_{DS}} I_{ds2}(L_1, 0)\,dx,$$

which is the condition of continuity of current in the channel at the boundary of M_1 and M_2. The above expression for drain-current is valid for linear region only. For saturation region, same equation 4.11 is used by replacing the normal channel length, L_g with reduced channel length ($L_g - l_d$) and V_{ds}

with V_{dsat} (derived in equation 4.12). Here, l_d is the distance by which channel length is shortened when V_{ds} increases beyond V_{dsat}, given by

$$\text{where } d_2 = V_{gs} - V_{th} + \phi_F,\ d_3 = \left(\frac{C_{ox}}{\varepsilon_{si}.E_c}\right)^2,\ d_4 = V_{fbf1} - V_{gs},\ A_1 = \frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{ox}}$$

$$c_1 = [d_3.d_4 + d_3.(V_x)],\ c_2 = \sqrt{1 + d_3.(d_4)^2 + 2.d_3.d_4.(V_x) + d_3.(V_x)^2} \times \sqrt{d_3},\ d'_4 = V_{fbf2} - V_{gs}$$

$$c_{11} = [d_3.d_4 + d_3.(V_{bi})], c_{22} = \sqrt{1 + d_3.(d_4)^2 + 2.d_3.d_4.(V_{bi}) + d_3.(V_{bi})^2} \times \sqrt{d_3},$$

$$c'_{11} = [d_3.d'_4 + d_3.(V_x)], c'_{22} = \sqrt{1 + d_3.(d'_4)^2 + 2.d_3.d'_4.(V_x) + d_3.(V_x)^2} \times \sqrt{d_3},$$

$$c'_1 = [d_3.d'_4 + d_3.(V_{bi})]\ c'_2 = \sqrt{1 + d_3.(d'_4)^2 + 2.d_3.d'_4.(V_{bi} + V_{ds}) + d_3.(V_{bi} + V_{ds})^2} \times \sqrt{d_3}$$

$$l_d = \sqrt{\frac{2.\varepsilon_o.\varepsilon_{si}}{q.N_a(y)}(V_{ds} - V_{dsat})}$$

$$I_{Dsat} = -2.W.v_{sat}.Q_{sat}(x) = 2.W.v_{sat}.C_{ox}(V_{gs} + V_{sub} - V_{th} + \phi_F - \phi(x))$$

$$V_{dsat} = \frac{1}{2.\alpha.\mu_s}\left(4.V_{th}.\mu_s - 2.\alpha.L_g.v_{sat} + 2.\sqrt{4.V_{th}^2.\mu_s^2 + \alpha^2.L_g^2.v_{sat}^2 + 2.\mu_s.\alpha.L_g.v_{sat}.(V_{gs} - V_{th})}\right) \quad (4.12)$$

Figure 4.6 shows the variation of drain-current (as calculated using equation 4.7) with drain-source voltage for different gate-source voltages for *DM DG* structure and *SM DG* structure. It is seen that the drain current in general increases when the gate metal work

function is higher. It is also observed that for smaller gate to source voltage, drain current is more or less same for both the structures.

In figure 4.6, the saturation drain voltage has been plotted against gate to source voltage for different values of channel length L_g . It is observed that saturation drain voltage is larger for large channel length for given gate to source voltages, as expected.

Figure 4.7 shows the drain current vs drain voltage characteristics for different doping distribution. It is seen that drain current is more in case of Pearson-IV distribution in comparison to other cases indicating that *DM DG* structure with Pearson-IV distribution allows for higher current capability.

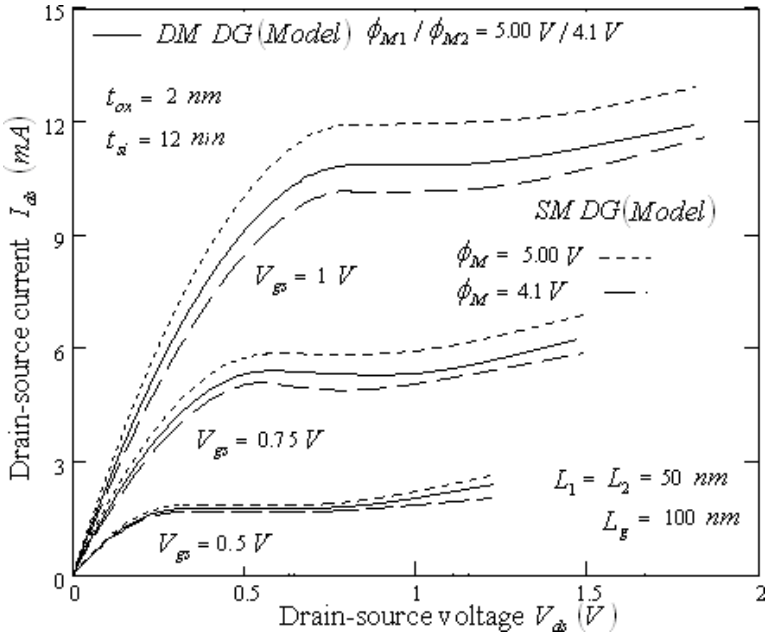

Figure 4.10: Drain-source current vs drain-source voltage for different gate-source voltagesin DM DG and SM DG SOI structures

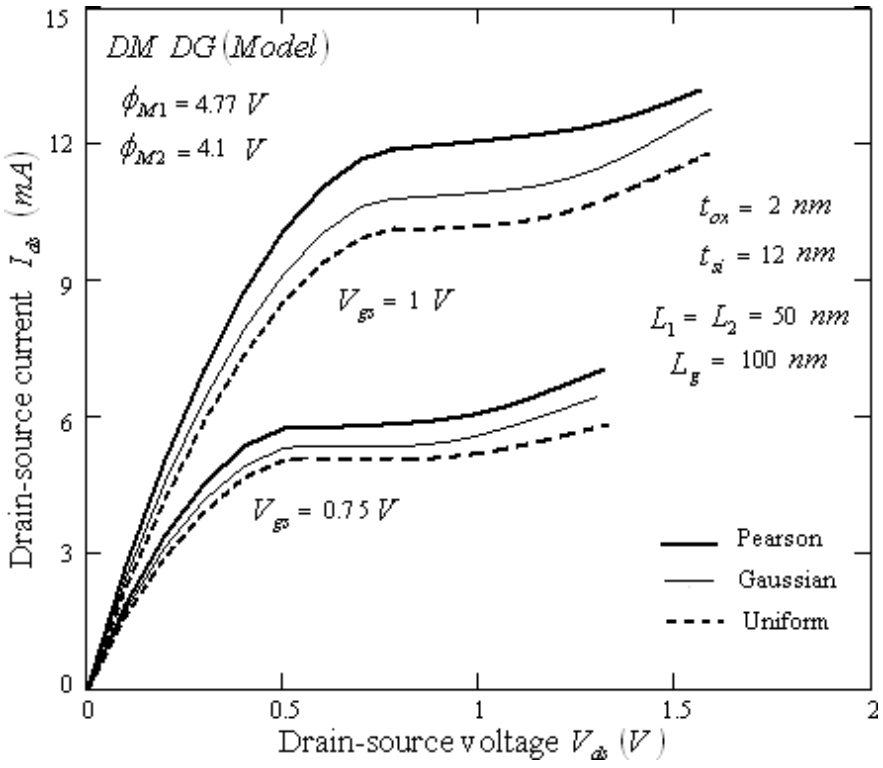

Figure 4.11: Drain-source current vs drain-source voltage characteristics in DM DG structure with different distribution functions

4.1.4 Transconductance

The transconductance of the n-channel DM DG FD SOI MOSFET is obtained by differentiating the drain-current with respect to gate-source voltage for a constant drain to source voltage and is expressed as

$$g_m = \left(\frac{dI_{ds}}{dV_{gs}} \right) \Bigg|_{V_{ds} = const.} \tag{4.13}$$

Using equation (4.7) the expression for g_m is derived as given below

$$g_m = \frac{2.W.\mu_{no}.C_{ox}}{L_1.(d_3)^{\frac{3}{2}}} \times (1 + A_1) \times \left[(d_2 + d_4).(c_{111}) + \left(\frac{c_1}{c_2} - \frac{c_{11}}{c_{22}} \right).\sqrt{d_3} \right] +$$

$$\frac{2.W.\mu_{no}.C_{ox}}{L_2.(d_3)^{\frac{3}{2}}} \times (1 + A_1) \times \left[(d_2 + d'_4).(c_{222}) + \left(\frac{c'_1}{c'_2} - \frac{c'_{11}}{c'_{22}} \right).\sqrt{d_3} \right]$$

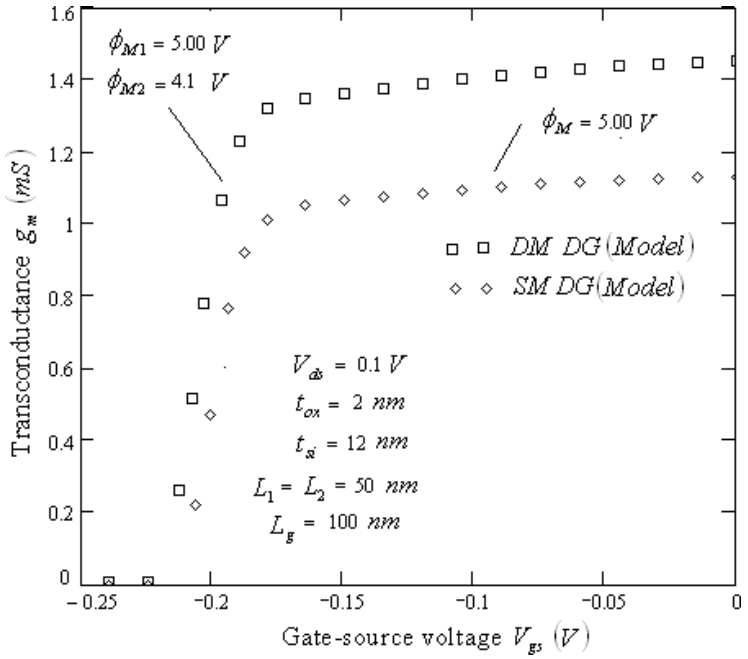

Figure 4.12: Transconductance vs gate-source voltage in DM DG and SM DG SOI structures for –ve gate to source voltage

Figure 4.8 and 4.9 show the transconductance vs gate-source voltage characteristics for*DM DG* and *SM DG SOI* structures. It is seen that transconductance is significantly largerin case of *DM DG SOI* structure indicating that the gate has better control over the conductance in case *DM DG SOI* structure.

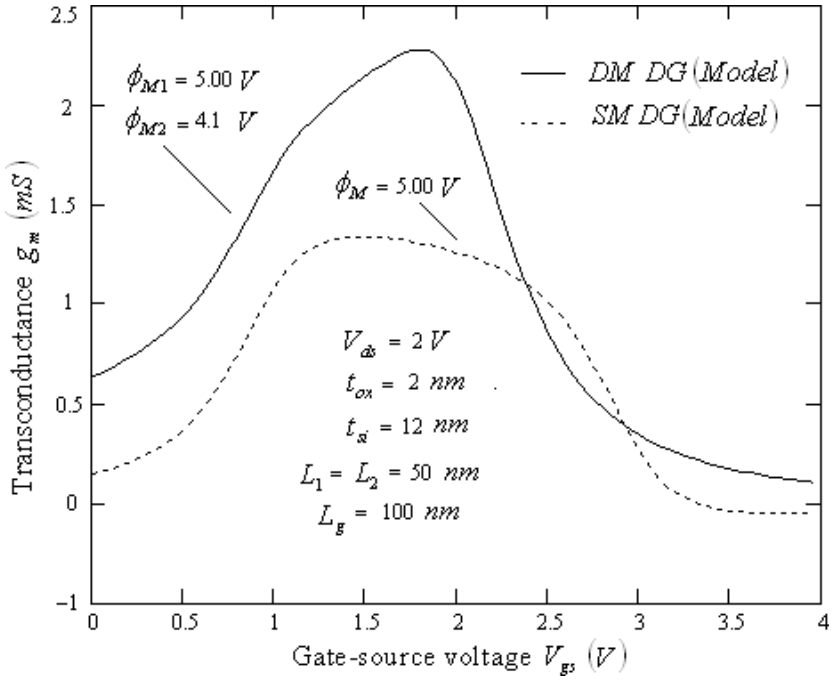

Figure 4.13: Transconductance vs gate-source voltage in DM DG and SM DG SOI structuresfor +ve gate to source voltage

4.1.5 Drain Resistance

Drain resistance (r_{ds}) is important for design of high frequency, low-voltage devices. It can be expressed as

$$r_{ds} = \left(\frac{dI_{ds}}{dV_{ds}} \right)^{-1} \Bigg|_{V_{gs} = const.} \tag{4.14}$$

Using equation 4.7, the expression for r_{ds} is derived to be,

$$r_{ds} = \frac{2.W.\mu_{no}.C_{ox}}{L_1.(d_3)^{\frac{3}{2}}} \times (1 + A_1) \times \left[(d_2 + d_4).(c'_{111}) - \left(\frac{c_1}{2.c_2} \right).\sqrt{d_3} \right] + \frac{2.W.\mu_{no}.C_{ox}}{L_{2.}(d_3)^{\frac{3}{2}}} \times (1 + A_1) \times \left[(d_2 + d'_4).(c'_{222}) + \left(\frac{c'_{11}}{2.c'_{22}} - \frac{c'_1}{2.c'_2} \right).\sqrt{d_3} \right] \tag{4.15}$$

The drain-resistance curve has been plotted against drain-source voltage for DM DG and SM DG SOI structures as computed in next chapter. It is observed that the drain-resistance in case of DM DG SOI structure is lower than that of SM DG SOI structure. This is consistent with higher current drive capability of the DM DG SOI structure. The drain resistance vs drain-voltage characteristics for different combinations of work functions of M_1 and M_2 is also plotted.

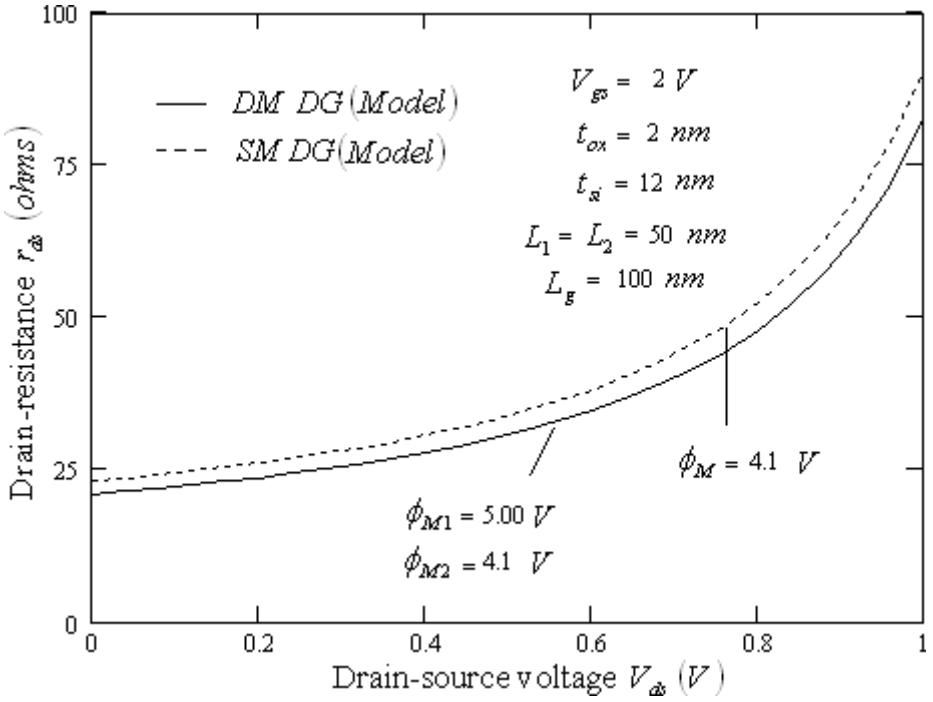

Figure 4.14: Drain-resistance vs drain-source voltage in DM DG and SM DG SOI structures

It is observed that as the work functions difference decreases the drain-resistance increases. Also, the drain-resistance vs drain voltage characteristics has been plotted, as computed from equation (4.15) and using device simulator ATLAS. The two characteristics are in very close agreement indicating the high accuracy of the analytical model. The plot of drain-resistance vs drain-voltage for different doping distribution. It is seen that the drain resistance is lowest in case of Pearson IV doping distribution.

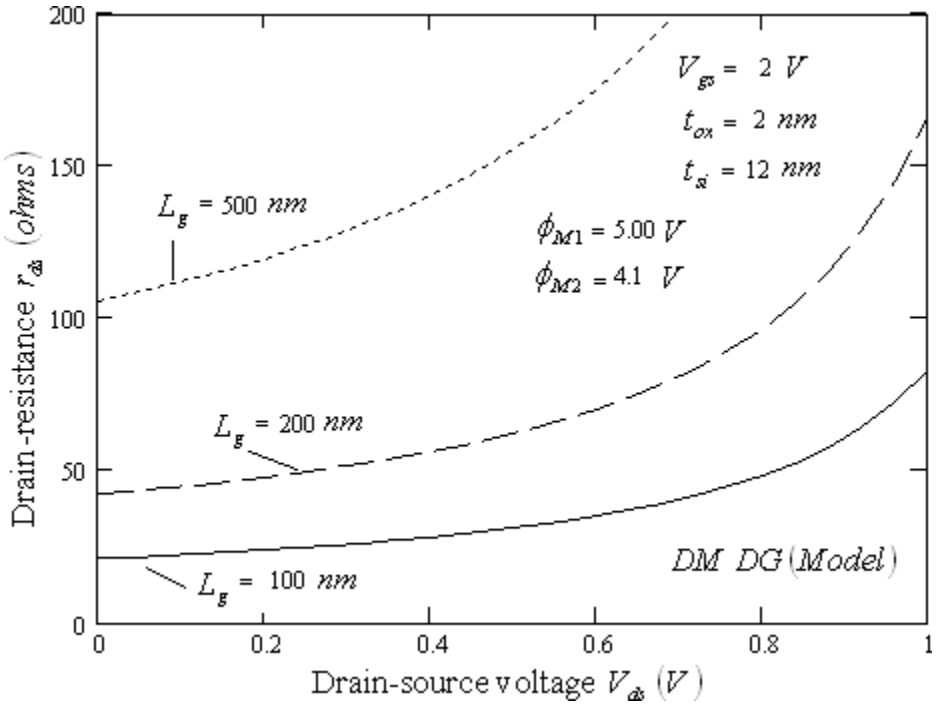

Figure 4.15 Drain-resistance vs drain-source voltage for different combinations of L_1 and L_2 inDM DG SOI structure

4.1.6 Cut-off Frequency

The cut-off frequency is one of the important figure of merit of low-voltage and high- speed devices. The cut-off frequency increases as the size of the device decreases. It is expressed as

$$f_c = g_m/2\pi L_g \, C_T \qquad (4.16)$$

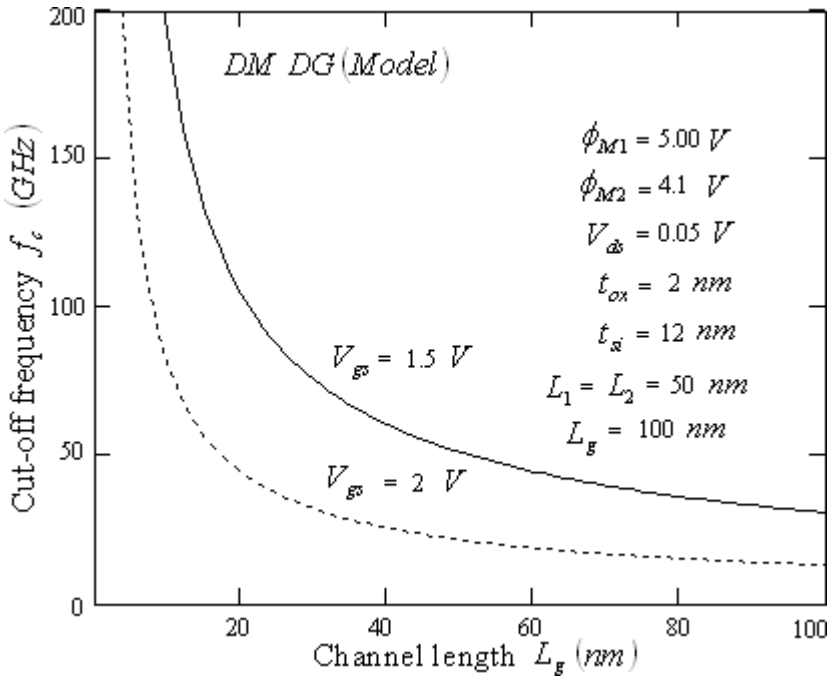

Figure 4.16: Variation of cut-off frequency along the channel-length for different gate-source voltages in DM DG SOI structure

where gm is the transconductance of the device, L_g is the channel-length (equal to L_1+ L_2) and CT is the total device capacitance. Figure 4.16 shows the plot of cut-off frequency vs channel-length for a given gate-source voltage for DM DG FD SOI MOSFETs as computed from the analytical model. It is seen that the cut-off frequency decreases as the gate to source voltage increases which is because of lower value of transconductance on higher gate to source voltage. Figure 4.17 shows a comparison between cut off frequency for DM DG and SM DG structures as computed using analytical model. It is seen that the DM DG structure offers higher cutoff frequency which is because of higher transconductance of DM DG structure.

Figure 4.18 shows the plot of cut off frequency vs channel length for DM DG structure as computed using analytical model and using device simulator ATLAS. The two curves are in very good agreement bringing out the correctness of the proposed analytical model. .

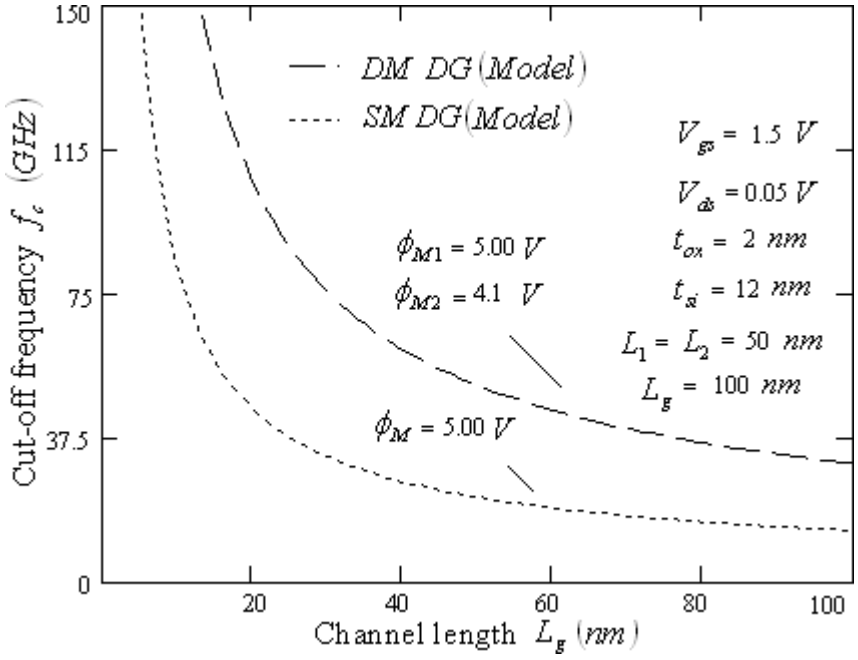

Figure 4.17: Variation of cut-off frequency along the channel-length in DM DGand SM DG SOI structures

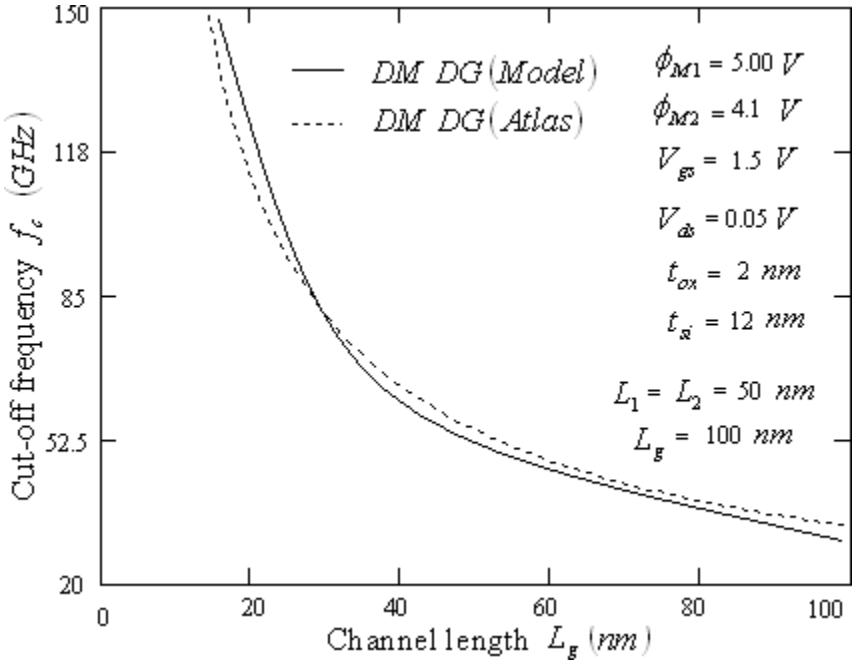

Figure 4.18: Comparison between analytical model and device simulator values for cut-offfrequency along the channel length in DM DG SOI structure

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION AND FUTURE SCOPE

The bulk *Si MOSFET* has been the main device forming the backbone of the developmentof ultra high-density ICs. However, due to continuous miniaturization, a situation has reached, where the performance parameters of the MOSFETs are degraded (due to the basic physical limits), to the extent that it is very difficult to fabricate ICs with nano-scalebulk MOSFETs. A new generation device, which can offer good performance parameters i.e. low power consumption and high speed, even for nano-sacle devices, is required. As discussed in Chapter-I, DG SOI MOSFET followed by dual-material (which offers improved electron transport efficiency), is one such alternative.

For IC design, it is essential to have an accurate device model describing the electrical behavior of the device. This require the exact solution of the basic semiconductor equation i.e. Poisson's equation, continuity equation, current transport equation and other related equations. The solution of these equations invariably involved numerical analysis.The situation becomes even more complex for nano-sacle devices where the equationsare to be considered in 2-D or 3-D. In such situations, an analytical model which can giveapproximately same results as may be obtained by exact numerical analysis would be very useful, provided the results obtained from the analytical model are same as those obtained by numerical solution within acceptable tolerance. Also, for improved device performance the body region is doped by ion implantation process. For this, the device behavior needs to be analyzed assuming a doping distribution as close to practically obtained doping distribution (i.e. Pearson IV) as possible.

In this work, attempt has been made to develop 2-D analytical models with Pearson IV type doping distribution for the following parameters of DM DG FD SOI MOSFET : potential distribution, electric field distribution, electron velocity distribution, subthreshold swing,

threshold voltage, device capacitance, drain-current, transconductance, drain resistance, cut-off frequency. The dependence of all these parameters on the drain to source voltage, gate to source voltage, channel length, impurity distribution in the silicon layer and the work function difference of the two metals has been studied using the proposed analytical model and also using device simulator program ATLAS.

It has been observed that

1. In case of DM DG SOI MOSFET, the source is effectively screened from the variation in the drain voltage due to step function profile of the potential at theinterface of metals M1 and M2. The electric field is reduced near the drain leading to reduction in hot carrier effect. The reduction in electric field nearthe drain is also found to be dependent upon the difference between the work function of the two metals. As the difference between the work functions of the two metal increases the electric field near the drain decreases.
2. The effect of DIBL is considerably reduced in case of DM DG SOI MOSFET.
3. The nature of impurity distribution also affects the potential and electric field distribution and therefore the device characteristics.
4. The peak electron velocity is higher in case of DM DG SOI structure in comparison to the same for SM DG SOI structure.
5. Better control on threshold voltage in case of DM DG SOI structure in comparison to the same for SM DG SOI structure for small channel lengths.
6. The depletion capacitance is much smaller in case of DM DG structure (in comparison to same for SM DG) particularly for a small value of gate to source voltage. This is expected because in SM DG structure the metal chosen had larger work function.
7. The drain current increases with increase in the gate metal work function difference.
8. Transconductance is significantly larger in case of DM DG SOI structure indicating that the gate has better control over the conductance in case DM DG SOI structure. It is also observed that larger the work functions difference larger is transconductance. The drain-resistance in case of DM DG SOI structure is lower than that in caseof SM DG SOI structure. This is

consistent with higher current drive capability of the DM DG SOI structure.

9. The cut-off frequency decreases with increasing channel length. The DM DG structure offers higher cut-off frequency because of higher transconductance of DM DG structure.

5.2 Future Scope of the Work

Different gate structures along with SOI wafer technology are now viewed as the most important emerging engineering technology for use in leading edge CMOS IC production during the next 3-5 years. One plausible scenario during this period is the rapid adoption of SOI wafers in place of single crystal silicon wafers now employed as starting substrates for high-end logic device (e.g., microprocessors) and SOC (**S**ystem **O**n **C**hip) applications at the 0.13 and 0.10 micron technology nodes. SOI technology appear to offer an excellent platform for integrating RF and digital circuits on the same chip due to its superior RF/ high speed performance.

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ANNEXURE

ANNEXURE 1 : PUBLISHED PAPER

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Performance Analysis and Characterization of Double Gate and Gate All Around MOSFET

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***Abstract*—The optimization and comparison of structure of double-gate MOSFETs and gate-all-around (GAA) MOSFETs was carried out. The fin width to gate length ratio and SCE (short channel effects) were discussed and studied. The 3-D simulations affirmed that while gate length was same as fin width, the short channel effects were inhibited. The ratio of the fin width to the gate length was maximized up to 1.2 in cylindrical channel GAA MOSFETs as compared to cubical channel ones.**

Keywords: MOSFET, GAA, Short Channel Effects, DIBL and Silvaco TCAD

I. Introduction

In CMOS for the sub-50-nm regime, Double-Gate (DG) MOSFETs, owing to good short-channel-effect (SCE) immunity and high transconductance, have been regard as most optimistic choice [1]. The ratio of fin width to the gate length is considered to be crucial design parameters, in order to have better DIBL (drain-induced barrier lowing) and SS (sub threshold swing) [2]. For proper inhibition of SCEs, fin width found to be 0.7 times less than the gate length [3]. Hence, fin width being the most crucial factor in determining the critical dimension, stands as a hindrance to aggressive scaling. The gate electrodes and the gate oxide envelop around the channel region in GAA (Gate All Around) MOSFETs. Fin width to the gate length ratio is increased while using GAA MOSFETs. Since the gate length is smaller than fin width, the SCEs are sufficiently minimized, if the design variable of GAA MOSFETs are optimized. In this work, double gate MOSFET and Gate All Around MOSFETs were quantitatively investigated by ratio of fin width to the gate length optimely. Initially, 30-nm DG and GAA MOSFET structures are introduced [4].

Multiple gate lengths, gate-oxide thickness, fin heights and fin widths were used to perform three dimensional simulations for DG and GAA MOSFETs to analyze short channel effects. Based on the results, the design optimization of GAA MOSFET was focused and was established that the GAA MOSFETs were optimized with cubical channel where all three parameters fin width, fin height and gate length were all equal [12-14].

II. Different Gate Structures

Short-channel effects appear when gate control is affected by electric field lines between drain and source [5]. Increasing the doping concentrations of the channel can minimize the effects of electric field lines that propagate through depletion regions, in a bulk device (figure 3A). However, as a result of large doping concentrations the proper functioning of small devices is hindered. Before reaching the channel majority of electric field lines, in FDSOI devices, go through buried oxide layer (Fig. 3B). By using thin BOX and ground plane under it, SCEs in FDSOI MOSFETs can be minimized (figure 3C). Increased junction capacitance and increased body effect, are the major drawbacks of the approach [6-10]. The electric field lines terminate at the bottom gate electrode in a double gate structure; hence a greater competent device structure is achieved. Figure 1 shown the different Gate structures. Equations 1 to 4 indicate DIBL and short channel effects in FDSOI and double gate.

FDSOI Drain Induced Barrier Lowering =

$$0.80[\varepsilon_{si}/\varepsilon_{ox}\ \{(1+t_{si}^2/L_{el}^2)t_{ox}/L_{el}(t_{si}+\lambda t_{BOX}/L_{el})\}V_{DS}] \quad (1)$$

FDSOI Short Channel Effects =

$$0.64[\varepsilon_{si}/\varepsilon_{ox}\ (1+t_{si}^2/4L_{el}^2)t_{ox}/L_{el}\{(t_{si}+\lambda t_{BOX}/L_{el})\}V_{bi}] \quad (2)$$

DG Drain Induced Barrier Lowering =

$$0.80[\varepsilon_{si}/\varepsilon_{ox}\ \{(1+t_{si}^2/L_{el}^2)t_{ox}/L_{el}(t_{si}/2L_{el})\}V_{DS}] \quad (3)$$

DG Short Channel Effects =

$$0.64[\varepsilon_{si}/\varepsilon_{ox}\ \{(1+t_{si}^2/L_{el}^2)t_{ox}/L_{el}(t_{si}/2L_{el})\}V_{bi}] \quad (4)$$

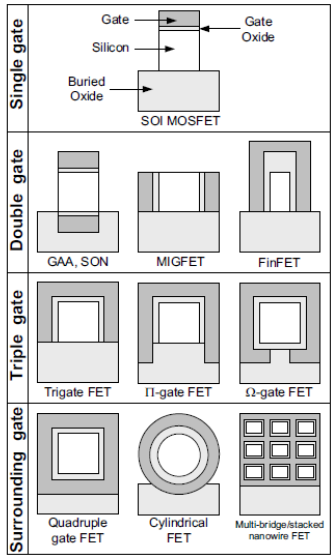

Fig. 1: Different Gate Structures

III. Result and Discussion

A. Optimization of GAA MOSFETs

Simulations for various gate-oxide- thickness and Fin height splits were conducted to optimize GAA MOSFETs' design parameters and reduce short-channel. Simulations were performed for1.5, 2, 2.5, and 3 nm gate-oxide thicknesses in the beginning.

It was observed that in both the devices, with reduction in the gate-oxide thickness DIBL gradually decreased. Taking into account the obstacles, the optimal gate-oxide thickness is set to 2 nm in the fabrication process. Even for the 30 nm Fin width, in case of gate oxide thickness of 2-nm, the DIBL stayed below 115 mV/V, as shown in Fig. 5. an additional notable thing in fig 6 was that in GAA MOSFETs, with 3-nm thick gate-oxide, the SS and DIBL characteristics were superior compared to 2nm thick gate oxide in DG MOSFETs. Thus, showing that, in respect of CMOS scaling GAA MOSFETs have an advantage. Fig. 8 shows DIBL and SS characteristics for 30, 35, 40, 45, and 50 nm fin heights, for both devices. The reduction in fin height resulted in improved SS and DIBL for GAA MOSFETs but remained same for DG MOSFETs. In case of GAA MOSFETs, due to increased controllability, owing to additional gates on the channel, reduction in fin height resulted in reduction of short channel effects. For relevant SS and DIBL, it was confirmed from the data, fin width can be same or larger than gate length.

B. Ideal Cylindrical-Channel MOSFETs

The design was optimized for GAA MOSFETs, as the gate length, the fin height, and the fin width were taken as 30 nm, and gate oxide thickness was 2nm, for proper inhibition of SCEs in previous simulation results. As a consequence, the GAA MOSFETs' performance had been improved with a cubical channel. DG MOSFETs generally do not suffer corner effects like GAA MOSFETs generally do. Reliability problem and the short-channel effects may arise, as the large electric field accumulate around each channel edges, thus channel cannot be evenly controlled by gates.

Summary of results is illustrated in Table 1-4. In the cubical-channel MOSFETs the electric fields are out of balance unlike ideal cylindrical channel MOSFET, where the gate electric field equally affects the channels, and hence OFF currents are notably reduced. Improvement of driving current was likely as the channel volume is enhanced that would lead to higher current flow. Due to increase in SS, OFF current became worse. DIBL and SS characteristics are shown in fig 12 with cylinder diameters. As it could be anticipated that cylinder diameter increase could cause the SS and DIBL to rise. In Fig 4 and 5, 84.8 mV/dec and 118.38 mV/V were the values of the SS and DIBL respectively.

Short channel effects were still minimized even when the gate length is smaller than cylinder diameter. For pertinent short channel effect, proportion of the cylinder diameter to the gate length could be increased to 1.2. Table 1-4 gate voltage vs g_m, gate length vs threshold voltage, Fin width vs Sub Threshold Swing characteristics and Fin width vs Drain Induced Barrier Lowering respectively. Figure 2-5 shows characteristics based on values obtained in table 1 to 4.

Table. 1: Gate Voltage vs Transconductance for Double Gate and Gate All Around Structure

S.No.	Gate Voltage (Volt)	Transconductance (g_m) (mS/µm)	
		g_m for DG	g_m for GAA
1.	-1	0	0
2.	-0.8	0	0
3.	-0.6	0	0
4.	-0.5	0	0
5.	-0.3	0	0
6.	-0.1	0.02	0.02
7.	0	0.04	0.04
8.	0.1	0.05	0.06
9.	0.3	0.06	0.09
10.	0.5	0.03	0.04
11.	0.6	0.02	0.03
12.	0.8	0.01	0.02
13.	1	0.01	0.02

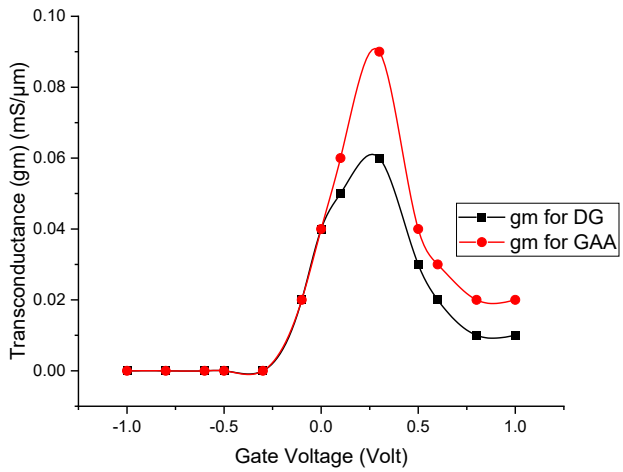

Fig. 2: Gate Voltage vs Transconductance for Double Gate and Gate All Around Structure

TABLE. 2: GATE LENGTH VS THRESHOLD VOLTAGE

S.No.	Gate Length (nm)	Threshold Voltage (Volt)	
		DG	GAA
1.	10	-0.215	-0.18
2.	20	-0.2	-0.16
3.	30	-0.18	-0.15
4.	40	-0.16	-0.15
5.	50	-0.15	-0.147
6.	60	-0.148	-0.146
7.	70	-0.146	-0.144
8.	80	-0.142	-0.14
9.	90	-0.14	-0.138
10.	100	-0.14	-0.135

TABLE. 3: FIN WIDTH VS SUB THRESHOLD SWING CHARACTERISTICS

S. No.	Fin Width (nm)	Sub Threshold Swing			
		DG (t_{ox}=2nm)	DG (t_{ox}=3nm)	GAA (t_{ox}=2nm)	GAA (t_{ox}=3nm)
1.	10	64	65	62	64
2.	12	64	66	63	65
3.	15	70	72	68	70
4.	18	72	77	70	72
5.	20	75	80	71	74
6.	23	77	85	74	76
7.	25	80	90	76	78
8.	28	82	97	78	80
9.	29	84	99	80	82
10.	30	90	105	82	88

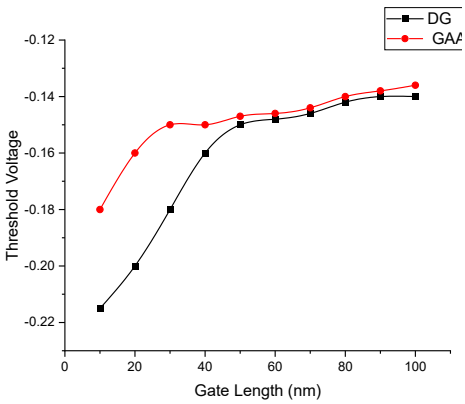

Fig. 3: Gate Length vs Threshold Voltage for Double Gate and Gate All Around Structure

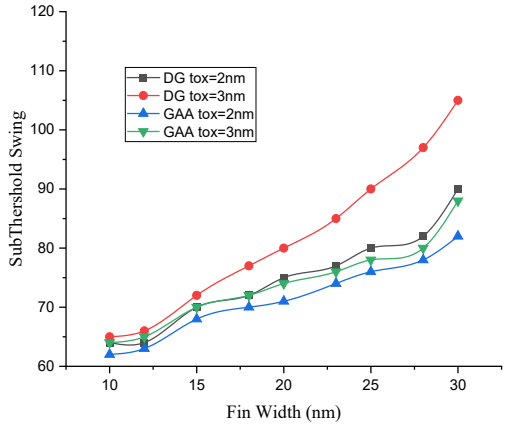

Fig. 4. Fin Width vs Sub Threshold Swing Characteristics for Double Gate and Gate All Around structure for Different t_{ox}

Drain Induced barrier Lowering (DIBL) = $\Delta V_{Th}/\Delta V_{DS}$

$=(V_{Th1} - V_{Th2})/(V_{DS1} - V_{DS2})$

ΔV_{Th}= Threshold Voltage

ΔV_{DS} = Drain to source voltage

TABLE. 4: FIN WIDTH VS DRAIN INDUCED BARRIER LOWERING

S. No.	Fin Width (nm)	Drain Induced Barrier Lowering (mV/V)			
		DG (t_{ox}=2nm)	DG (t_{ox}=3nm)	GAA (t_{ox}=2nm)	GAA (t_{ox}=3nm)
1.	10	29	32	20	28
2.	12	41	48	25	40
3.	15	49	59	34	48
4.	18	52	65	45	51
5.	20	60	77	50	56
6.	23	80	90	52	65
7.	25	92	115	60	70
8.	28	105	130	68	82
9.	29	120	180	76	86
10.	30	140	240	80	95

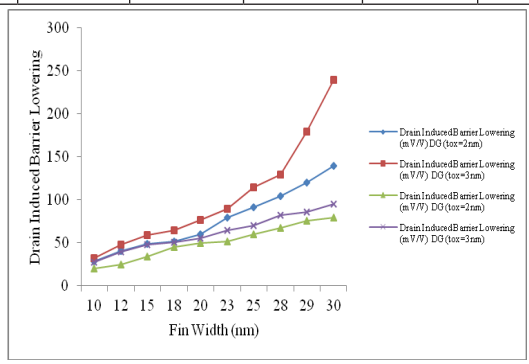

Fig. 5: Fin width vs Drain Induced Barrier Lowering for Double Gate and Gate All Around Structure for Different t_{ox}

IV. Conclusion

The cylindrical-channel MOSFETs', simulations were performed. The Ideal cylindrical-channel MOSFETs with reduced corner effects compared to cubical-channel GAA MOSFETs had smaller SS and DIBL. Hence, it was observed that the cylindrical-channel could be employed for optimized GAA MOSFET structure and the short-channel effects were suppressed. However, the gate length is smaller than fin width in this ideal cylindrical-channel MOSFET with 1.2 as the maximum ratio of the fin width to the gate length.

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