Dissertation

on

Performance Evaluation of Opamp with High supply Rejection in 180 nm CMOS Technology

Submitted in partial fulfillment

for the award of degree of

MASTER OF TECHNOLOGY

in

Electronic Circuits and Systems

Submitted By:

Akhtar Saleem Ansari

(6001140340)

Under the Guidance of

Mohd. Amir Ansari

(Supervisor)

Dr. Piyush Charan

(Co-Supervisor)

Department of Electronics & Communication Engineering.

INTEGRAL UNIVERSITY, LUCKNOW

May-2022

DECLARATION

This is to declare that I, Akhtar Saleem Ansari have completed the M.Tech Dissertation work on the topic "**Performance Evaluation of Opamp with High supply rejection in 180 nm CMOS Technology".** The work embodied in this Dissertation is my own bonafide work carried out by me under the supervision of **Mr. Mohd. Amir Ansari** (Supervisor) and **Dr. Piyush Charan** (Co-Supervisor) at Integral University, Lucknow. The matter embodied in this Dissertation has not been submitted elsewhere for the award of any other degree/diploma. I declare that I have not willfully lifted up some other's work, para, text, data, results, etc. reported in the journals, books, magazines, reports, dissertations, thesis, etc., or available at web-sites.

Date:

Place: Lucknow

Signature

Akhtar Saleem Ansari

Enrollment No.:6001140340

CERTIFICATE

This is to certify that **Akhtar Saleem Ansari** has carried out the research work presented in the dissertation entitled **"Performance Evaluation of OpAmp with High supply rejection in 180 nm CMOS Technology"** for the award of Master of Technology (M.Tech.) in Electronic Circuits and Systems from Department of Electronics and Communication Engineering, Integral University, Lucknow under my supervision. To the best of my knowledge, the contents of this dissertation have not been submitted to any other institute or university for the award of any degree.

Signature of Supervisor

Full Name: Mr**.** Mohd. Amir Ansari

Designation: Assistant Professor

Address: Dept. of ECE, Integral University

Date:

Place: Lucknow

Signature of Co-Supervisor

Full Name: Dr. Piyush Charan

Designation: Assistant Professor

Address: Dept. Of ECE, Integral University

Date:

Place: Lucknow

ACKNOWLEDGEMENT

First of all I would like to thank **Almighty Allah**, the most Beneficial Graceful and Merciful, for being the source of my strength, in spite of all the stress and troubles. I have been blessed by Almighty Allah with some extraordinary people who supported me throughout my M.Tech journey. Words can never be enough in expressing how graceful I am to those incredible people in my life who have made this dissertation possible to me.

First and foremost, my debt of gratitude is extended to my Guide **Mr. Mohd. Amir Ansari,** Asst. Professor and Co-Guide **Dr. Piyush Charan,** Asst.Professor, Department of Electronics and Communication Engineering for their gentle encouragement, brilliant suggestions and relaxed demeanor made for a good working relationship throughout this project work.

I am grateful to **Dr. Syed Hasan Saeed**, Professor and Head, Department of Electronics and Communication Engineering for providing necessary facilities in the department. I am also thankful to **Dr. Shailendra Kumar,** Associate Professor, M.Tech coordinator for his consistent support throughout the semester.

My Special thanks to **Dr. Imran Ullah Khan**, Associate Professor, Department of Electronics and Communication Engineering for his great support to complete my course. His support gave me strength every time.

I am grateful to my **parents** and my **wife** for their immense support. I can honestly say it was their constant prayers to complete my work.

At last , reaching major milestones in one's life doesn't happen without the assistance of great many people, and for each one them I am truly blessed and grateful. I expressed my thanks to all those who directly or indirectly helped me in this academic endeavor.

I also apologize for lacuna during course, all of which were quite unintended but complete mine.

Date: Signature

Place: Lucknow Akhtar Saleem Ansari

Enrollment No.:6001140340

ABSTRACT

This dissertation work details the designing process of two silicon two-stage operational amplifiers with indirect feedback compensation and with Miller compensation technique. The main objective of this thesis is to study the advantages of high supply rejection phenomenon in Op-Amp applications with Miller compensation and how this technique can be applied to meet certain design specifications. The operational amplifiers are designed with 180 nm CMOS process ideally for temperature range of 25°C to 300°C. The Op-amp is designed to have a DC gain of about 70 dB and phase margin of 60^{o}. The Miller compensation technique; showed a reduction in the compensation capacitor size, meaning a smaller design area, and an improvement in the phase margin from the LHP zero. Also, the proposed design showed a higher unity gain frequency. Further analysis of indirect feedback frequency compensation on multistage amplifiers (greater than two) should be conducted to analyze the potential of this compensation method under more complex compensation against the commonly used Miller technique.

The operational amplifier has been designed and simulated using Tanner EDA (SPICE Platform) in 0.18 μm (or180 nm) CMOS -1.8 V process technology. The phase margin achieved is 57^{o} with the slew rate of 24 V/μs. The seemingly compromise of the slew rate is all due to the targeted high phase margin which lower the response speed hence slew rate of the amplifier. The designed and implemented two stage operational amplifier also achieved high PSRR of -94.66 dB, which again promises a remarkable performance in the noisy and supply-fluctuating environment.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LISTOFABBREVIATION

S.No.	Abbreviation	Name
1	Opamp	Operational Amplifier
2	PSRR	Power Supply Rejection Ratio
3	CMRR	Common Mode Rejection Ratio
4	SIBO	Single Input Balanced Output
5	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
6	NMOS	N-Channel MOSFET
7	PMOS	P-Channel MOSFET
8	SCE	Short Channel Effects
9	DIBL	Drain Induced Barrier Lowering
10	GBW	Gain-Bandwidth Product
11	SR	Slew Rate
12	OTA	Operational Transconductance Amplifier

CHAPTER 1

INTRODUCTION

Operational Amplifiers are one of the indispensable blocks of modern integrated systems and are used in wide varieties of circuit topologies like data converters, filters, references, clock and data recovery circuits. However, continued scaling in CMOS processes has continuously challenged the established paradigms for operational amplifier (op-amp) design. As the feature size of CMOS devices keeps shrinking, enabling yet faster speeds, the supply voltage is scaled down to enhance device reliability and to reduce power consumption.

1.1 Background

Operational Amplifiers (Op Amps) are an integral part in design of various analog and mixed-signal systems. Their applications extend from dc bias applications to high speed ADC/DAC's and filters. General purpose Op Amps find their use in most analog subsystems, particularly in switched capacitor applications [1]. In most of such systems, the overall system performance is strongly influenced by the Op Amp performance. With major enhancements in computer aided design (CAD) tools, advancements in semiconductor characterization and modeling, transistor scaling, and the progress of fabrication processes, the integrated circuit field is expanding rapidly [2]. Integrated circuits once served the role of subsystem components, portioned at analog-digital boundaries, however they now integrate complete systems on a chip by combining both analog and digital functions. Complementary metal-oxide semiconductor (CMOS) technology has been the main-stay in mixed-signal because it provides density and power savings on the digital side, and a good mix of components for analog design. Scaling down of CMOS feature sizes enable yet faster speeds, the supply voltage is scaled down to enhance device reliability and improve power consumption [1].

1.2 Basics of Op-Amp Design and Design Challenges

Operational amplifiers are linear devices that have all the properties required for nearly ideal DC amplification and are therefore used extensively in signal conditioning, filtering or to perform mathematical operations such as add, subtract, integration and differentiation. An Operational Amplifier, or op-amp for short, is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the resulting function or "operation" of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of "Operational Amplifier".

1.2.1 Introduction to Op-Amp basics

An Operational Amplifier is basically a three-terminal device which consists of two high impedance inputs. One of the inputs is called the Inverting Input, marked with a negative or "minus" sign, (–). The other input is called the Non-inverting Input, marked with a positive or "plus" sign (+), as shown in *Figure 1.1.*

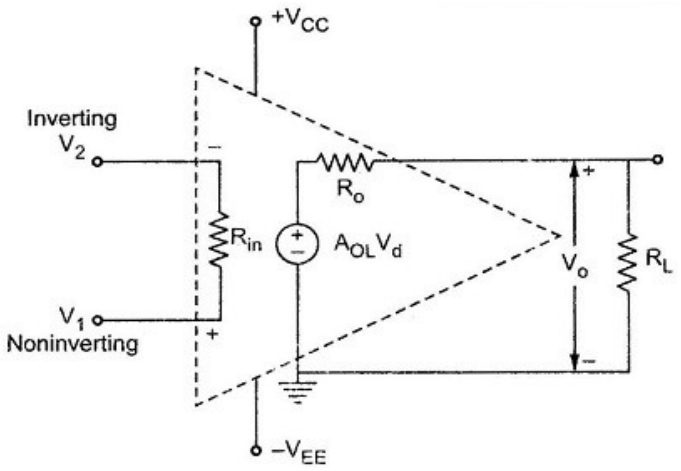


Figure 1.1: Op-Amp practical model

A third terminal represents the operational amplifiers output port which can both sink and source either a voltage or a current. In a linear operational amplifier, the output signal is the amplification factor, known as the amplifiers gain (A) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.

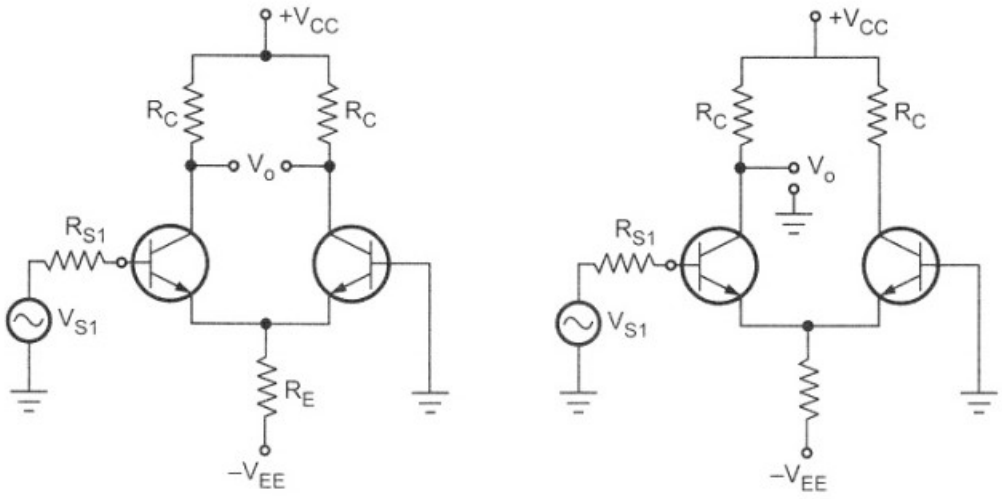
- Voltage – Voltage "in" and Voltage "out"
- Current – Current "in" and Current "out"
- Transconductance – Voltage "in" and Current "out"
- Transresistance – Current "in" and Voltage "out"

Since most of the circuits dealing with operational amplifiers are voltage amplifiers, we will limit the tutorials in this section to voltage amplifiers only, (V_{in} and V_{out}).The output voltage signal from an Operational Amplifier is the difference between the signals being applied to its two individual inputs. In other words, an op-amps output signal is the difference between the two input signals as the input stage of an Operational Amplifier is in fact a differential amplifier as shown in *Figure 1.1*.

Differential Amplifier as an integral component

The circuit below shows a generalized form of a differential amplifier with two inputs marked V1 and V2. The two identical transistors TR1 and TR2 are both biased at the same operating point with their emitters connected together and returned to the common rail, -Vee by way of resistor Re.The circuit operates from a dual supply +Vcc and -Vee which ensures a constant supply. The voltage that appears at the output, Vout of the amplifier is the difference between the two input signals as the two base inputs are in anti-phase with each other.

So as the forward bias of transistor, TR1 is increased, the forward bias of transistor TR2 is reduced and vice versa (Figure 1.2). Then if the two transistors are perfectly matched, the current flowing through the common emitter resistor, Re will remain constant.Like the input signal, the output signal is also balanced and since the collector voltages either swing in opposite directions (anti-phase) or in the same direction (in-phase) the output voltage signal, taken from between the two collectors is, assuming a perfectly balanced circuit the zero difference between the two collector voltages.



(a) (b)

Figure 1.2: (a) Single Input Balanced Output**(b)** Single Input Unbalanced Output

This is known as the Common Mode of Operation with the common mode gain of the amplifier being the output gain when the input is zero. Operational Amplifiers also have one output (although there are ones with an additional differential output) of low impedance that is referenced to a common ground terminal and it should ignore any common mode signals that is, if an identical signal is applied to both the inverting and non-inverting inputs there should no change to the output. However, in real amplifiers there is always some variation and the ratio of the change to the output voltage with regards to the change in the common mode input voltage is called the Common Mode Rejection Ratio or CMRR for short.

Operational Amplifiers on their own have a very high open loop DC gain and by applying some form of Negative Feedback we can produce an operational amplifier circuit that has a very precise gain characteristic that is dependent only on the feedback used. Note that the term “open loop” means that there are no feedback components used around the amplifier so the feedback path or loop is open.

An operational amplifier only responds to the difference between the voltages on its two input terminals, known commonly as the “Differential Input Voltage” and not to their common potential. Then if the same voltage potential is applied to both terminals the resultant output will be zero. An Operational Amplifiers gain is commonly known as the Open Loop Differential Gain, and is given the symbol (A).

1.2.2 CMOS technology, scaling and power challenges

Over the last six decades, scaling down of MOSFETs in size is continually been done so as to accommodate more devices in a given area of the chip. According to Moore’s law “the number of transistors on integrated circuits doubles approximately every 2 years”, whose prediction proves to be true and helps to set targets for research and development of semiconductor devices. The International Technology Roadmap for Semiconductors

(ITRS) is used to identify the obstacles and shortcomings so that industries and research communities can work effectively to overcome these shortfalls and helps in building semiconductors of future generation. Key findings as well as predictions of ITRS (2013) include:

(i) Combination of 3D architecture of the device as well as devices with low power would dominate in the new world of scaling which is coined in short as "3D Power Scaling." by stacking transistors in multiple layers increasing number of transistors per unit area can be accomplished.

(ii) Emergence of carbon nanotubes, graphene combinations which offer ballistic conductors may be witnessed in the next decade.

(iii) CMOS platform with extended functionality by heterogeneous integration of novel technologies and inventing devices with new processing paradigms can give new opportunities to semiconductor products of future era.

Over the past four decades, there has been an increasing trend in the power consumption oflead microprocessors. In 1974, NMOS was preferred to PMOS due to its advantages like speed and area, in the carrier mobility aspect. But due to lower noise margins and static power consumption (DC) of NMOS technology, it was no longer used in the industry from 1980s. CMOS technology exhibits low intrinsic power dissipation and superior scaling characteristics and hence dominated IC industry in 1980s. But the rate at which chip area grows is much smaller as compared to the rate at which the number of transistors as well as power density grows. Hence the temperature of microprocessors increases as a result of increased power consumption. These temperatures may even exceed $120^{o}\,C$ these days. As the temperature increases to higher levels, there would be an increase in leakage power which in turn increases the total power consumption. This can even cause thermal runaway in extreme situations.

$$P_{static} = I_{LEAK} \,.\, (\text{Supply Voltage}) \qquad (1.1)$$

where P_{static} is the static power dissipation, I_{LEAK} is the sum of the leakage currents of MOSFET in OFF state.

$$P_{dyn} = f \cdot C_L \cdot (\text{Supply Voltage})^2 \quad (1.2)$$

where f is the frequency, C_L is the load capacitance. It is seen that if supply voltage is not scaled down, there will be an increase in power density. Increase in power thus results in reduced battery life, more heat production and proves to be economically and environmentally less friendly. So, there is a significant challenge posed due to power consumption in designing IC systems. Various setbacks posed by scaling conventional MOSFETs are:

- Channel Length Modulation
- Short Channel Effects (SCEs)
- Velocity Saturation of Carriers
- Drain Induced Barrier Lowering (DIBL) and Punch Through
- Surface Scattering
- Impact Ionization
- Hot-Carrier Injection
- Narrow Channel Effect
- Subthreshold Conduction

Hence conventional *MOSFETs* cannot be looked upon as the device of future semiconductor world as it can be optimized to a certain limit only. The subthreshold swing of conventional *MOSFETs* have a minimum limit of 60 *mV/decade*. MOSFETs have I_{ON} to I_{OFF} ratio in the order of 10^3 to 10^4. So, device engineers go forward with nonconventional devices with subthreshold swing less than 60 *mV/decade* and higher I_{ON} with very negligible I_{OFF} trying to make them behave as ideal switch.

1.2.3 Op-Amp Design Trends and Challenges

The single stage amplifiers are inherently stable and typically have excellent frequency response assuming the gain bandwidth is ten times higher than the single pole. However, single stage amplifiers suffer from low dc gain and is even less for submicron CMOS transistors. In general, Op Amps require at least two gain stages which introduce multiple poles in the frequency response. The poles contribute to the negative phase shift and may cause $\angle FA$ to reach -180° before the unity gain frequency. Therefore due to insufficient phase margin the circuit would oscillate. Thus the amplifier circuit needs to be modified to increase the phase margin and stabilize the closed loop circuit. This process is called" compensation". By intuition, two different approaches may be taken to stabilize the loop [1, 3].

The more straightforward approach way is make the gain drop faster in order for the phase shift to be less than -180° at the unity gain frequency. This approach achieves stability by reducing the bandwidth of the amplifier and the most popular pole splitting method uses this procedure. Another compensation method pushes the phase crossover frequency out by decreasing the total phase shift. In this particular case the total number of poles needs to be reduced while still maintaining the dc gain. This is achieved by introducing zeros into the open and close loop transfer function to cancel the poles, or using feed-forward paths to improve the phase margin without narrow-banding the bandwidth as much as the pole splitting does.

One of the major requirements for an Op-Amp is sufficiently big open loop gain and wider bandwidth, which generally is quoted under an important qualitative parameter as gain-bandwidth product (*GBW or* f_T *or GB* simply). The excessive high input impedance, low output impedance, high slew rate (SR) and high-power supply rejection ratios (PSRR) are additional benefits one could like to achieve to implement an optimum performing Op-Amp. These amplifiers are key factors of maximum of the analog subsystems, especially in ASP and switched capacitor filters' applications. For couple of decades, a CMOS implementation of analog circuits proved better than its contrary circuits in other technologies and with different configurations like Operational transconductance

amplifiers (OTA). In order to obtain higher overall performance, MOS transistors used in Op-amp design are scaled down, which facilitates incorporation of more quantity of transistors on identical chip. The non-forestall growth in processing capability in step with chip and working frequency is result of scaling. Scaling down of CMOS feature sizes allow yet faster speeds, the deliver voltage is scaled all of the way right down to decorate tool reliability and enhance electricity intake. A conventional two stage amplifier consists of a high gain (gm) differential amplifier stage followed by a single input common source stage connected via miller compensating capacitor to improve upon the stability in terms of Phase Margin.

(a) Parallel Compensation

Parallel compensation is a classical way to compensate the Op Amp. A capacitor is connected in parallel to the output resistance of a gain stage of the operational amplifier to modify the pole. It is not commonly used in the integrated circuit due to the large capacitance value required to compensate the Op amp, which considerable die area.

(b) Pole Splitting – Single Miller Compensation (SMC)

The most widely used compensation technique in analog circuit and systems design is undoubtedly pole splitting. A miller capacitor is used to split the poles, which causes the dominant pole to move to a much lower frequency and thus reducing the bandwidth and providing ample stability. This method is featured in the original 741/101 bipolar OpAmps designed by Robert Widlar and was widely implemented henceforth [4].

Ideal operational amplifiers are functional blocks that have infinite voltage gainover an infinite bandwidth, infinite input resistance and zero output resistance. In practice, op amps only approach these ideal characteristics. They use negative feedback to establish and control a closed-loop transfer function that is stable and independent ofthe open-loop

gain of the op amp. *Figure 1.3* presents a functional block diagram of a basic operational amplifier. The differential input stage provides the required high gainfor the op amp and can also perform the differential-input to single-ended output

conversion.

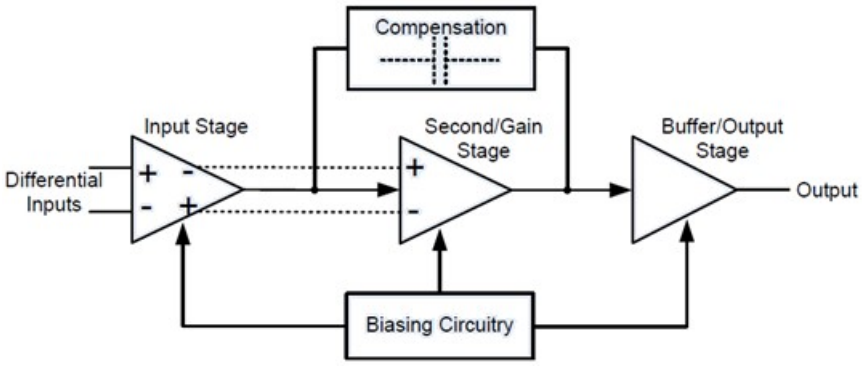


Figure 1.3: Basic operational amplifier

The second stage is usually an inverting stage and can offer high gain as well as differential-to-single ended conversion if necessary. Op amps that need to drive small resistive loads also include a buffer/output stage that drives the load and determines the output swing. The compensation circuitry ensures frequency stability when the op amp is used in a negative feedback network. The biasing circuitry provides a stable, quiescent operating point for the entire circuit. Op amps with different levels of complexity are used in many applications and it is important to understand the parameters used in evaluating these op amps. A brief review of the op amp parameters is included here.

The dynamic range of an op amp is controlled by the op amp's offset voltage, noise, input common-mode range (ICMR) and output swing. The ability of the op amp to provide an accurate closed-loop gain is dictated by the open-loop gain (A_{OL}). The frequency response of the circuit is characterized by the small-signal bandwidth, phase margin, settling time and also large signal bandwidth. The range of maximum and minimum voltages that can be obtained without any clipping at the output is represent eds output swing. Slew Rate is the maximum rate at which the output voltage can change. The ability

of an op amp to prevent its output from being affected by any variation in the power supply voltage is characterized as PSRR. The factors that influence these parameters are examined in detail in the subsequent chapters.

Although basic gain equation of op-amp models the majority of the major error sources of the Op-Amp; the expression falls short of listing other important errors such as distortion, bandwidth, slewrate, linearity, etc., which are also considered as key performance characteristic parameters of amplifiers. Despite this, the equation still fairly depicts a good picture of the most important DC parameters of an Op-Amp, in particular the offset and offset-related parameters. The errors associated with the input bias currents (the voltage drop across the source resistances of the signal sources at the input terminals of the Op-Amp) are mostly encountered in Op-Amp swith bipolar junction transistors (BJT's) at the input stage.MOS transistors do not have a *DC* bias current at their inputs, since they are voltage-controlled devices with capacitive elements at the input. Therefore the sixth and seventh terms of Eq. (2.1)are removed in a *DC* analysis if MOS devices are used for the input differential pair of the Op-Amp. Throughout this dissertation, and in designing of low offset amplifiers via a new technique called "Dynamic Offset Cancellation", the focusing will be on using MOS devices as the primary choice of device.

When offset reduction is realized with a method that affects all the offset errors, the *DC CMRR* can be defined as the ratio of the change in the offset voltage due to a change in common mode voltage. It is then clear that offset performance affects the *CMRR* parameter. The same is also true for *DC PSRR*, which is then defined as the change in offset voltage due to a change in supply voltage. The above are represented by the fourth and the fifth terms of Eq. (2.1).The noise term at low frequencies is called flicker noise, also known as 1/f noise. This error is often summed up or treated as part of the DC offset error, as it is frequently indistinguishable from the offset error itself. The second term of Eq. (2.1) represents the input-referred error due to the finite DC open-loop gain of the Op-Amp. As this *DC* gain is normally very high, the effect of the error in a closed-loop circuit of low or moderate gains is usually negligible; especially when compared to the offset

error itself. As an example to see the relative weight of different error terms, we consider a rail to rail Op-Amp with a MOS differential pair at the input stage, with an input referred offset error of 10mV, *CMRR* of 80dB, *PSRR* of 60dB, and DC open loop gain of 10,000. If the amplifier is used in system with a 5(1 ± 10%) V power supply, the error terms associated with Common mode change, supply change, and finite gain are 0.5mV, 1mV, 0.5mV respectively. The larges terror source is still an order of magnitude less than the offset alone. This example shows that the offset error by far dominates the other error sources in MOS amplifier design.

1.3 Literature Survey

Operational amplifier is most versatile and essential building block in analog signal processing (ASP) and RF CMOS integrated circuits of modern world wireless applications. The operational amplifier (Op-Amp) has an excessive benefit due to the direct coupled multiple stages of voltage amplifier with a differential input and, single or differential output to be used with negative feedback. One of the major requirements for an Op-Amp is sufficiently big open loop gain and wider bandwidth, which generally is quoted under an important qualitative parameter as gain-bandwidth product (*GBW* or f_T or *GB* simply). The excessive high input impedance, low output impedance, high slew rate (SR) and high-power supply rejection ratios (PSRR) are additional benefits one could like to achieve to implement an optimum performing Op-Amp. These amplifiers are key factors of maximum of the analog subsystems, especially in ASP and switched capacitor filters' applications. For couple of decades, a CMOS implementation of analog circuits proved better than its contrary circuits in other technologies and with different configurations like Operational transconductance amplifiers (OTA).

In order to obtain higher overall performance, MOS transistors used in Op-amp design are scaled down, which facilitates incorporation of more quantity of transistors on identical chip. The non-forestall growth in processing capability in step with chip and working

frequency is result of scaling. Scaling down of CMOS feature sizes allow yet faster speeds, the deliver voltage is scaled all of the way right down to decorate tool reliability and enhance electricity intake. A conventional two stage amplifier consists of a high gain (gm) differential amplifier stage followed by a single input common source stage connected via miller compensating capacitor to improve upon the stability in terms of Phase Margin. One such topology has been shown in Figure 1.4, where A1 is the first high gain stage of a differential amplifier and A2 is a standard common source amplifier with moderate gain and high current driving capability. Cc acts as a miller capacitance providing pole- splitting for stability improvement.

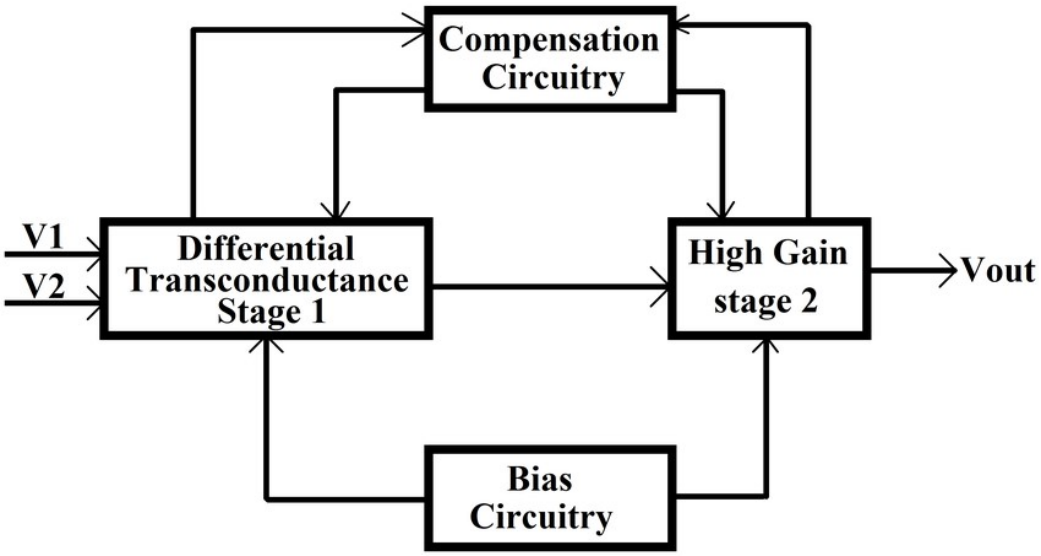


Figure 1.4: Conventional Two-stage Miller compensated Op-Amp topology

A simple technique with adaptive load is used in [5] to achieve class-AB operation; however, a high SR is not achieved (SR ~ 1.58 V/µs). This is because the maximum output current depends on the maximum source-gate voltage of the output PMOS transistor which cannot go close to lower rail V_{SS}. In addition, GBW = $g_m/(\pi Cc)$ has only a factor of two increase compared to the GB of the conventional Miller op-amp. The structure in [6] has

the same problem of low CE (SR). This is due to the fact that it uses current starved CMOS inverters as output stages. From the point of view of GBW, scheme in [6] performs as a conventional two-stage Miller op-amp without g_m, A_{OLDC}, and GB enhancement. It also does not provide a high PM. The op-amp in [7] has class-AB operation while focusing on lowering the supply voltage using the body-driven technique [7, 8, 9, 10, 11]. In body driven op-amps, the bulk transconductance (g_{mb}) is usually a factor 4–5 lower than the gate transconductance (gm). This degrades the GBW, DC open-loop gain (A_{OLDC}), and also leads to higher input-referred noise, offset, etc. In addition, for relatively moderate swings a p-n junction in the well of the input transistors can turn ON and increase significantly the input leakage current. The class-AB circuit in [12] has the ability of driving moderately high capacitive loads but its stability is provided by three compensation capacitors and resistors which increase essentially the complexity and area requirements. In addition, slew rate does not have a high value (SR = 6.4 V/μs) for the same reason as in [9]. Another disadvantage of [9]–[11] and [15, 16] is that they are not capable to drive a very wide range of capacitive loads which is rather important in applications such as peak detectors, micro-electromechanical systems (MEMS), liquid-crystal displays (LCDs), and line drivers [13, 14, 15]. Kavyashree, 2017 [16] supplied the layout of -level operational amplifier (Op Amp) in 90 nm CMOS technology for better compensation. The design consists of a smaller number of transistors; therefore, the implementation is area optimized. Achieved open loop gain of the amplifier is seventy 54.89 dB. The gain bandwidth (GBW) is 7 MHz. The phase margin is 48^o degree with a 10 pF capacitive and 1 MΩ resistive load. S. Goyal, 2015 [17] also worked with the continuous developing smaller transistor channel length, designing of immoderate normal overall performance analog incorporated circuits.

The op amp is core unit of the analog and mixed signal circuit. Integrated operational amplifier not only has the normal function of the amplifier, it can be a linear operation, comparison and waveform generation functions of the analog signal. Thus, as the continuous development of integrated circuit technology, high-performance operational amplifiers used in A / D converter, D / A converter, Bandgap reference circuits,

Comparator circuits and other systems. Op-amp circuit performance has a direct impact on overall system performance. An article in 2012, Yang Guanga and Yu Bin [18] designed an operational amplifier based on TSMC 0.35μm CMOS process. Using folded cascode and the two class AB output structure. Using HSPICE 2004 software for circuit simulation. Simulation results show that the designed circuit has high gain and low static power consumption. Another paper [19] describes the design of miller compensated two stage operational amplifier operating at 3.3V for the continuous time delta sigma modulator applications. The design mainly focused to achieve sufficient electrical characteristics such as unity gain frequency, slew rate, Input common mode range, output swing and output offset all are taken into consideration as power consumption is secondary concern.

In a work by Priyanka,H S Aravind, Yatheesh in 2017 [20] design and implementation of two stage operational amplifier operating at *2.9V to 3.7V* power supply at *180 nm CMOS*t echnology is presented. The proposed two stage op amp produces high gain. Design and simulations results are verified using CADENCE tool. This design has accomplished a high power supply rejection ratio (PSRR) greater than -80db and other performance parameters such as input common mode range (ICMR), common mode rejection ratio (CMRR) and slew rate is verified. The presented work simulation results have been obtained by *180nm CMOS* technology. After the simulation, in ordered to optimize the better performance most of the transistors size still needed to be modified. The advantages of two stage op-amp have good gain, high output swing, low noise and good bandwidth over folded cascode. And it needs compensation, low PSRR value compared to folded cascode. Now a day design of an operational amplifier is to get high gain and simultaneously optimizing all process parameters has become mandatory.

A highly power-efficient class-AB–AB Miller op-amp is discussed in a recent work by Shirin Pourashraf and Jaime Ramirez-Angulo [21]. The structure uses gm enhancement based on local common-mode feedback to provide class-AB operation with enhanced effective gm, open-loop gain, unity-gain frequency, and slew rate (SR) without significant increase in quiescent power consumption. Utilization of a nonlinear load leads to large

symmetric positive and negative SRs. Stability over an extremely wide range of capacitive loads is achieved through a combination of Miller and phase-lead compensations. The unity-gain frequency does not show sensitivity to capacitive load values a composite class-AB-AB Miller op-amp is presented that has high CE (SR), essentially improved BW and A_{OLDC} (both over factor 10), and the ability to drive a very wide range (over four decades) of capacitive loads starting from relatively low C_L values and maintaining a constant f_{UG}, high *PM* approximately insensitive settling time to C_L loads. This is achieved by using a combination of Miller and phase-lead compensations with a C_L–independent pole–zero cancelation. The op-amp uses LCMFB to boost the effective g_m, the SR, and the dynamic output current of the first stage. A study of the non-inverting amplifier based on a two stages CMOS un buffered current-feedback-amplifier (UCFOA) is also proposed in another recent paper by HerveBarthelemy, Remy Vauche and Valentin Gies [22]. Using a small-signal equivalent circuit (macro-model) of the non-inverting amplifier, a theoretical explanation of the closed loop gain is given. The op-amp phase margin and its bandwidth have been estimated from the quality factor Q of resonance and using a novel description of the UCFOA input stage called *Operational Transconductance Conveyor (OTC)*. The *OTC* description can be viewed as an extension of *type II* second generation current conveyors. Based on the fundamental parameters of the proposed *OTC,* a theoretical approach given in this paper explains how to evaluate precisely the value of the *UCFOA* compensation capacitance. PSPICE was used to simulate both the theoretical macro-model and the *CMOS* configuration from a *0.35µm typical BSIM3V3* transistor models.

1.4 Motivation and Objective of the Work

Operational amplifiers (op amps) are versatile devices used as key functional blocks in a variety of high-precision analog/mixed-signal systems. Its application spans the broad electronic industry filling requirements for signal conditioning, special transfer functions, analog instrumentation, analog computation and special systems design [23].

Various design aspects of compensated Op-amp have been analyzed and worked upon to come up with the optimized solution in this dissertation work. The major motivation and objectives for the proposed work are as following:

- ***Compact Design solution with high package density:***

There continues to be a growing interest in developing SoC (System-on-Chip) integrated systems for use in numerous applications. These applications often place challenging constraints in the design of various electronic components. "Extreme environments" represent a class of niche electronic applications wherein the electronic components must operate in an environment that is outside the domain of commercial or military specifications. This would include temperatures above or below the standard military specification, in a radiation intensive environment such as space, in a high vibration environment, in a high (low) pressure environment, or even in a caustic or chemically corrosive environment as inside the human body [24].

- ***Robustness against temperature and supply variations:***

In this dissertation, noise and temperature effects on op-amp design have been studied and a robust operational amplifier that works across a supply fluctuations has been designed and simulated for performance evaluation. With the recent development of low temperature electronics to support space exploration, this work is targeted at the moon's surface environment where the ground temperature swings up to *393 K (120 °C)* during the day and down to *93 K (-180 °C)* during the night. At present, robotic exploration rovers [25] have all the essential parts that control the system, such as electronics, batteries and computers operating in a temperature controlled environment of a warm electronic box (WEB). The temperature in the WEB is maintained to be within the operating range of all the enclosed components in order to guarantee their reliable operation. Heaters, thermostats, heat switches and gold paint help maintain the temperature inside the WEB, but they increase the system's power consumption, size and mass [25].

With this motivation, the goal of this work is to develop an operational amplifier that functions well under extreme temperatures. This would help in designing remote electronic systems for robotic rovers and other spacecraft that provide data acquisition and control for various applications.

1.5 Methodology of the proposed work

Numerous design techniques and CMOS operational transconductance amplifiers(OTAs) and Op-Amps architectures are investigated and an efficient frequency compensation and high PSRR methodology for the realisation of two stage op-amp is identified. The requirement of high PSRR and high stability (Phase Margin) is addressed and two stages are proposed. The high-frequency performance of these equalisers is studied in detail and OTA non-ideal effects are compensated using a new set of design equations as well as independent electronic tuning of equaliser parameters. To investigate the practical performance of Op-amps and differential amplifiers, a fully-differential amplifier and single stage common source is implemented using a commercial *0.18 µm n-well CMOS* process.

In addition to high PSRR of fully differential amplifiers, this dissertation investigates the frequency compensation approach in the design of two stage op-amp structures. The first stage is capable of producing CMRR and high gain. To approach for a design which is being targeted for the low power and high speed aspects, a lot of circuital architectures will have to be simulated and analysed. To solve the purpose, a high potential Circuit simulator tool will be required. Following is the list of some such tools:

- **Simulator environment: SPICE (schematic level):**
  - TANNER T-SPICE will be extensively used for circuital design and validation.
  - ADS (Advance Design System from Keysight Technologies)

- **Technology/model files:**

Depending on the advancement of the circuit, corrosponding Technology (CMOS and/or Bipolar) and Device model files will be required, which will be then used for the simulation purposes. Some technical specifications which may be required for the work are as follows:

- CMOS/BJT models (Level 49 and above)
- 3.3 V and below supply levels
- 180 nm, 90nm and 35nm

1.6 Scope of the Dissertation

The purpose of this work is to design an operational amplifier that can operate in extreme environments. Specifically, the op amp is targeted to serve as a general purpose building block in high-precision analog signal conditioning systems. There are several parameters that characterize an op amp. Some key parameters include gain, gain-bandwidth, slew rate, input common-mode range (*ICMR*), common-mode rejection ratio (*CMRR*), power-supply rejection ratio (PSRR), output swing, offset voltage, noise and power consumption. Depending on the system specification, some characteristics are given more precedence over others. For this work, it is important that the gain, gain band width, output swing, noise and offset voltage are maintained at an acceptable level across temperature. The op amp is designed and simulated in *a 0.18-µm 1.8-V CMOS process*, under *SPICE (TSPICE from Tanner-EDA)* environment.

An all-*CMOS* approach is used for this work to provide the opportunity to study and analyze the impact of temperature variation on *MOS* devices and its influence on Opamp performance. An analysis of the common-mode feedback circuitry implemented in the differential input stage of the op amp is also performed.

The speed and settling accuracy of modulators are determined by the performance of the operational amplifier. The speed of the modern Data converters and modulators is determined by the unity gain frequency and settling time while the settling accuracy is determined by the DC gain of the op amp. In Switched-capacitor circuits charge being transferred from one capacitor to another rapidly in each clock of operation therefore
Op-amp slew-rate limit has to be taken into another design consideration. The Slew rate and bandwidth limitations produce harmonic distortion reducing the total SNDR of the modulators. In typical switched capacitors, the unity gain bandwidth of the operational amplifier, a general rule of thumb is that the clock frequency should be 5 times than the unity gain frequency and the phase margin is at greater than 70 degrees to ensure stability.

1.7 Organization of the Dissertation

The complete dissertation presented here consists of total 5 chapters including this one as chapter 1 (INTRODUCTION). The complete hierarchy of the upcoming chapters chronologically is as following:

Chapter 2 starts with a brief review of op amps. This is followed by a discussion on the influence of power supply and temperature on the operation of MOS devices, circuits and the constraints set on the design of extreme temperature op amps. The chapter mainly provides all the essential theoretical details of the Op-Amp developments like gain, frequency response, stability and compensation.

Chapter 3 provides an in-depth look at the design of the general-purpose op amp. The common-mode feedback circuit, the frequency compensation technique and current reference circuit are discussed. The proposed architecture with complete design information is presented along with design steps. Then, the op amp is characterized using simulation results.

Chapter 4 presents the simulated results from the proposed design of op amp and also describes the test setup used for each simulation environment. The simulated results are then compared with the theoretically estimated results.

Chapter 5 summarizes the overall development of the work, starting from theoretical conceptualization to final design and simulated results. It also provides major conclusions and the dissertation ends with a discussion of possible enhancements and future work.

CHAPTER 2

FUNDAMENTALS OF OP-AMP DESIGN

Operational amplifiers (OpAmps) are basic building blocks of a wide range of analogue and mixed signal systems. Basically, OpAmps are voltage amplifiers being used for achieving high gain by applying differential inputs. The gain is typically between 50 to 60 decibels. This means that even very small voltage difference between the input terminals drives the output voltage to the supply voltage. In the case of using 180 nm CMOS technology, this small voltage difference can be around tens of milivolts. As new generations of CMOS technology tend to have shorter transistor channel length and scaled down supply voltage, the design of OpAmps is a challenge for designers. In this chapter, an ideal OpAmp will be introduced. Later the performance parameters of OpAmp will be defined and then OpAmp's imperfections, which stems from the trade-offs between the parameters, will be briefly discussed. Following a review of simple topologies of OpAmp and a comparison between them, two techniques for achieving higher gain and output swing will be described. For the sake of simplicity, the OpAmp model used in this chapter is a single-ended operational amplifier with differential inputs. This chapter presents a detailed discussion on the design and implementation of the high gain general-purpose op amp. It begins with an analysis of the different stages used in the op amp’s architecture. Then, the complete schematic is presented and the performance parameters of the op amp are derived. The next section presents the simulation results that are verified with the hand calculated values.

2.1 Ideal Op-Amp

In the past, most Op-Amps were designed to be used in many applications. This means that they have been designed as general purpose building blocks. This property leads to the idea of an ideal Op-Amp with very high gain, high input impedance and low output impedance

disregard for the signal applied to the input. The transparent symbol for an ideal Op-Amp is shown in the Figure 2.1.

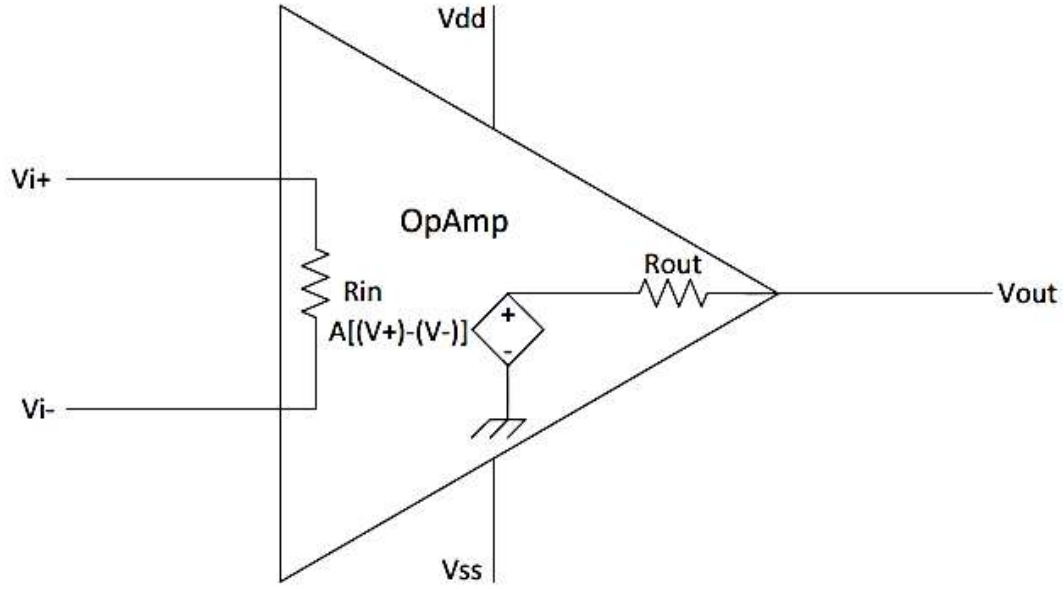


Figure 2.1: Ideal OpAmp

The Ideal OpAmp's properties:

- Infinite open-loop gain, $A_{ol} = \infty$
- Infinite input impedance, $R_{in} = \infty$
- Infinite slew rate
- Infinite bandwidth
- Infinite Common-mode rejection ratio (CMRR)
- Infinite Power supply rejection ratio
- Zero output impedance, $R_{out} = 0$
- Zero input current
- Zero input offset voltage (i.e., if $V_{i+} = V_{i-} \rightarrow V_{out} = 0$)
- Zero noise.

In practice, an Op-Amp with zero and infinitive parameters cannot be realized. There are always limitations (e.g., maximum output voltage swing) and trade-offs between the parameters (e.g. the trade-off between open-loop gain and speed) that should be considered during the design process. As a result, there need to be an appropriate specification for each application to device a compromise acceptable for all parameters.

2.2 Real Op-Amp

As mentioned in previous section OpAmps cannot be perfect. Due to the circuitry limitations and trade-offs that exist in analogue design there are a number of imperfections in OpAmps which are going to be briefly discussed.

(a) Finite Gain

Open-loop gain is finite in real operational amplifiers. Typically, Op-Amps exhibit open-loop DC gain between 50dB to over 60dB (Op-Amps with 130dB DC gain have been reported [14]). The loop gain of Op-Amp placed in a negative feedback loop is large enough, even with typical DC gains, that the circuit gain within the 3-dB bandwidth will be independently determined by the gain of the negative feedback.

(b) Finite Input Impedance

The assumption of infinite input impedance of the Op-Amps stems from the assumption of zero input current for the MOSFETs. Typically, the input impedance of the operational amplifier designed with MOSFETs is within the range of 100 to 1000 Mega Ohms.

(c) Non-Zero Output Impedance

Coming to the output impedance, Op-Amps can be thought of as voltage sources with internal resistance. The voltage drop across the output impedance of the Op-Amp causes

power dissipation and delivers less power to the load. The situation is getting worse as the load impedance of the amplifier decreases. However, the use of negative feedback topologies in most applications comes to designer's assistance. Negative feedback lowers the output impedance and reduces output errors accordingly. Typical output impedance for the open-loop operational amplifiers is in the range of 25-100 Ohms which will be much lower when using the Op-Amp in the negative feedback topology (almost a few Ohms). So, the assumption of zero output impedance is quite fair.

(d) Output Swing

Obviously output voltage of the operational amplifier cannot reach to the supply voltages level because of the transistors' overdrive voltages. An amplifier with voltage swing that allows output signal to go very close to supply voltages is called rail-to-rail amplifier. The need for larger output swing for application like high resolution data converters stems from the necessity of high SNDR and Dynamic Range for such circuits. The output swing limits the linearity of the circuits, especially in low voltage applications. One way to reach high output swing is to use fully differential Op-Amps.

(e) Input Current

Input current of the Op-Amps includes biasing current and leakage current of the input transistors. Input current for the MOSFETs is much smaller than BJTs or JFETs and it is about a few Pico amperes. Assuming symmetric circuit and matched input current, error will not be introduced to the differential output of the OpAmp but it shows itself as a DC offset and limits the output swing. An OpAmp with a high CMRR can help reducing the offset. Unfortunately neither the circuit is symmetric nor are the input currents matched. In reality, the input currents could differ by 10 percent or more which produces error to the output voltage that cannot be tolerated in some applications. The majority of the error could be corrected by the aid of adding a DC path (Ex. through a resistor) to the ground.

(f) Input Offset Voltage

One would expect zero output voltage when applying zero volts to the inputs of a differential amplifier, which is not the case in real amplifiers. The error voltage is caused by some imperfection and mismatches in the internal transistors and resistors of the Op-Amp and can be summed up as a DC voltage source and applied in series to one of the inputs of the Op-Amp. The input offset voltages can vary from microvolts to mili-volts depending on the circuit design and technology. CMOS technology has higher input offset voltage than Bipolar. In open-loop, due to very high voltage gain of the amplifier, input offset voltage brings the output to its saturation, even though the input voltage is zero. In negative feedback configuration the offset voltage will be amplified along with the input signal, introducing error to the output. This error can be problematic in applications with high precision DC amplification such as high resolution ADCs with very small LSBs (683.6 microvolts for 10-bit ADC and 341.8 micro volts for 12-bit ADC with1.4 volt peak-to peak differential input voltage). A major problem regarding to offset voltage is the voltage drift due to temperature change. This problem will be addressed under temperature effects headline.

(g) Common-Mode Gain

In An ideal operational amplifier, common-mode gain is zero and the amplifier amplifies only the differential input signal. However, in real amplifiers the voltages that are common to both inputs are amplified to some extent. This amplification is due to imperfections in tail current sources and mismatches between the transistors and resistors of differential pair. The standard measurement factor created to be used when comparing differential circuits is CMRR which can be calculated using this Equation 2.1:

$$CMRR = |A_{DM}/A_{CM}| \quad (2.1)$$

(h) Power-Supply Rejection

As opposed to the ideal case, supply noises play an important role in real amplifiers. Thus, the performance of amplifier in presence of supply ripples is of concern to many applications, especially mixed-signal applications that often deal with noisy digital supply lines. There is a factor called PSRR which stands for power supply rejection ratio that determines the ability of OpAmps to reject the changes in the power supply.

(i) Noise

Noise exists in amplifiers similar to all analogue circuits. The amount of noise puts a specification for minimum input on the requirement list of the amplifier. If the input signal would be less than this minimum, then it cannot be processed safely. This noise mostly consists of thermal noise and flicker noise of the devices in the circuit. Some of these devices contribute more than others, for example input transistors of the OpAmp. Those devices should be taken care of by widening and applying more bias current. There is a trade-off between maximum output swing and noise. In order to have more swing, with the same bias current, the overdrive of the transistors can be lowered to allow more swing. As the overdrive voltage goes down, the transconductance of the Amplifier increases which causes more drain noise current. For application s with demands on higher gain or bandwidth, noise becomes an important issue.

(j) Finite Bandwidth

The OpAmp gain calculated at DC will not stay the same at higher frequencies. As the operational frequency of the circuit increases the gain decreases. At first the gain drop is not significant to be considered as system failure, but after the 3-dB frequency the change in DC gain cannot be ignored. In the Figure 2.2 the gain characteristic of an OpAmp is plotted.

High frequency behavior of the OpAmp is critical for many applications, especially for those who need high precision gain like the OpAmp hired in a MDAC. The unity-gain frequency of the operational amplifier, "*fu*" the frequency in which gain drops to zero dB, is a good measure of small-signal bandwidth. Today, using CMOS technology, unity-gain frequencies larger than 1GHz can be achieved.

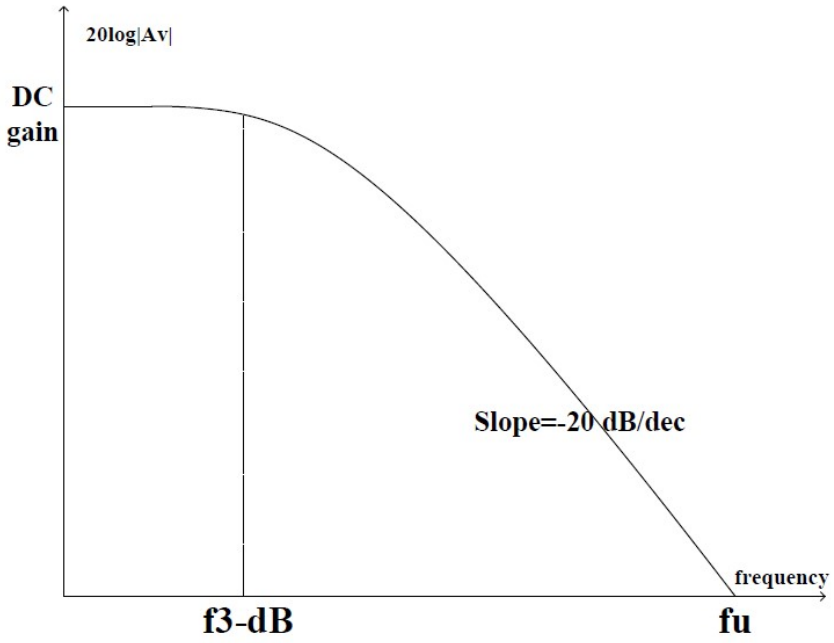


Figure 2.2: Gain versus Frequency

(k) Nonlinearity

Nonlinearity exists in all analogue circuits including OpAmps. There are several sources that introduce nonlinearity to the circuit. Transistors of the circuit can be considered as one of the main sources as they are inherently nonlinear devices. This source's impact on nonlinearity can be controlled by choosing larger transistor or higher overdrive voltage, especially for input transistors which play a significant role in this case. Considering power

and area requirements for circuits, one should be cautious about using these approaches on a large scale. Another source of nonlinearity is the output swing of OpAmps. The output voltage is limited between a minimum and maximum value near the supply voltages. When the output voltage crosses these boundaries, mostly due to high voltage gain, saturation occurs and causes output signal damage. Slewing can be considered as one of the other sources of nonlinearity. Reaching the maximum changing rate, the OpAmp's output voltage will not follow further voltage increase of the input. Internal capacitances are responsible for this effect. The problem can be partly remedied using fully differential circuits in order to suppress second-order harmonics. Furthermore, having higher open-loop gain helps the circuit to have more linearity in closed-loop system.

(l) Stability

The phase difference between input and output leads to oscillation if it becomes 180 degrees in a closed-loop configuration. This means that the amplifier is not stable. Even if the amplifier is stable, it can suffer from ringing which will affect settling time of the OpAmp. To measure stability of an amplifier, the concept of phase-margin comes to assist. PM is defined as the phase difference between 180˚ and the phase at the frequency in which the loop-gain ($\beta H(\omega)$) of the amplifier drops below unity. For PMs above 60 degrees, the step response of the feedback system shows a negligible ringing which provides fast settling time. Higher values of PM, gives more stable systems but not necessarily faster settling time. For large signal operation, there are other effects that should be considered, such as slewing, output swing and nonlinear behavior of devices in the circuit in presence of large changes in biasing voltages and currents in the circuit. Therefore, time domain simulations of closed-loop system are more efficient for measuring stability, bandwidth and settling time behaviour of the system.

(m) Drift

Parameters of semiconductor devices change due to time and temperature changes, resulting in a variation in OpAmp's parameters like: input bias current, offset voltage, etc. these variations are called drift.

(n) Slew Rate

The maximum rate of change of the OpAmp's output is called slew rate. It also means the maximum available current to charge the load capacitor. Slew rate is specified in volts per microsecond (V/μs) and is measured applying a large step to the input and using Equation 2.2:

$$SR = \frac{dV_{out}}{dt} = \frac{I_{\max}}{C_L} \tag{2.2}$$

When applying a step to the amplifier's input, the step response of the feedback system is proportional to the final output voltage of the system. Therefore, when applying larger steps to the input the output change rate will increase, up to the point where the amplifier enters slewing phase. In slewing phase the load capacitor will be charged by the maximum available current in output stage and the change rate will remain constant (SR).Figure 2.3 explains the concept of slewing. It can be seen that increasing the input voltage level wouldn't increase the output change rate after a certain level.

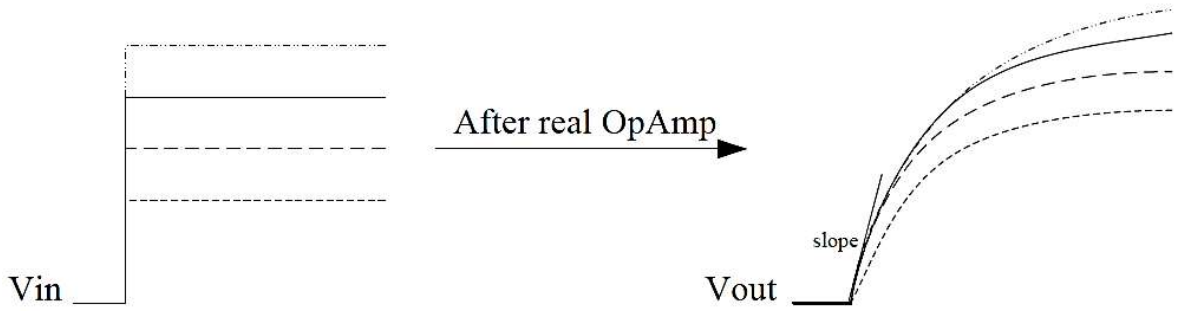


Figure 2.3: *Slewing Concept*

(o) Power Considerations

The output current of the OpAmp should be limited to a safe level so as not to damage the OpAmp and following circuitry. The output current also flows though the output impedance, generating heat and increasing temperature. So, if the temperature rises beyond the tolerance of CMOS device, it may cause thermal shutdown or even destroy the OpAmp.

2.3 Op-Amp Architecture

The design of an op amp is an iterative process which involves determining an appropriate architecture, designing the device sizes followed by analysis and simulation of the circuit to ensure that all specifications are satisfied. The specifications listed in Table 1.1 are examined in detail to determine the architecture. Although a specific value of open-loop gain is not included in the requirements, it is necessary to design the op amp with a high gain. This is done in order to ensure good closed-loop gain accuracy. Therefore, a two-stage architecture is employed for this op amp.

Table 2.1: Design Specifications

Parameter	Specification
I_{DD}	< 2 mA
Gain Bandwidth	> 1 MHz
Capacitive Load	50 pF
$ICMR_{MIN}$	0 V
Slew Rate	> 2 V/µsec
V_{OS}	< 10 mV
e_{ni} at 100 KHz	< 100 nV/√Hz
O/P swing for $\lvert I_{LOAD}\rvert = 0.3$ mA	$\geq (0.2 \rightarrow 3.1)$ V

2.3.1 Input Stage

Generally, the choice of architecture for input stage is dictated by the requirements set by noise, input common-mode range and gain. With this design being targeted to be operable across a wide temperature range, it is desirable to use an architecture that is simple enough to meet the specifications and is not constrained too much by temperature variation. Some topologies that could be used for the input stage include simple differential stage, differential-cascode and folded-cascode. From these choices available, the topology that is most favorable to meet the specifications is employed for the design.

While cascoding in the differential input stage increases the output impedance and thus helps in achieving higher gain, there is a reduction in the input common-mode range because of the extra voltage required by the cascode devices. Thus achieving a ground-sensing ICMR would not be possible with a differential-cascode input stage. In the folded-cascode topology, the direction of the signal from the input to the output devices is reversed and this offers good ICMR and wide output swing. By virtue of cascoding, high gain and good PSRR is also realized in this topology. The drawback of using this topology is that the addition of devices for folding increases the noise of the circuit. Also, the load pairs carry more quiescent current. Further, at low temperature operation where the threshold voltage of devices increase, the presence of cascade devices adds additional constraints to already low

voltage headroom available for the devices. Therefore, a simple differential topology as shown in *Figure 2.4* is utilized in the input stage of the op amp.

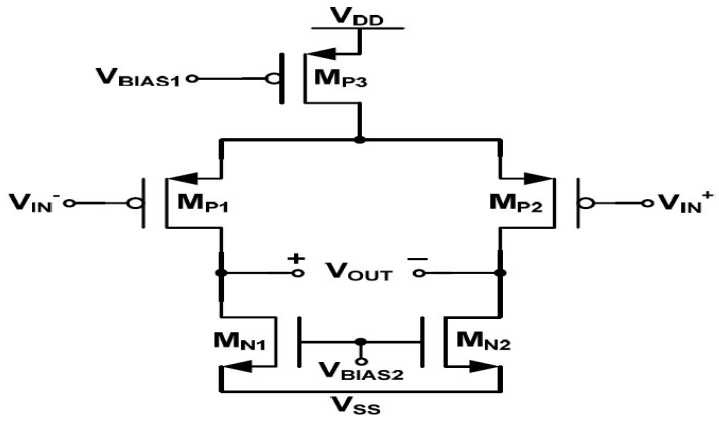


Figure 2.4: Input stage of the op amp

In order to meet the specification of ground-sensing ICMR, a PMOS-input differential pair is used. Using PMOS input devices also provides 2-5 times lower flicker noise when compared to NMOS pairs because the lower hole mobility reduces the number of carriers being trapped in surface states. Also, careful sizing of the input pair with respect to the load devices is required to lower the circuit's thermal noise. The noise component of the load devices is scaled by the ratio of their transconductance to that of the input pair devices. So, the gm of the input differential pair needs to be larger than that of the load pair in order to ensure low input referred noise. The common- mode (CM) output voltage of this differential-output input stage is not well-defined and is sensitive to mismatch and component variations. In order to maximize the output swing, this CM voltage needs to be stabilized at the mid-point between the signal swings. This is achieved by using a common-mode feedback (CMFB) loop that sets the CM level to a fixed reference voltage by means of a negative feedback.

2.3.2 Output Stage

The important criteria for designing an output stage are good current driving capability, low power dissipation, the ability to provide voltage gain and good stability by avoiding additional parasitic poles.

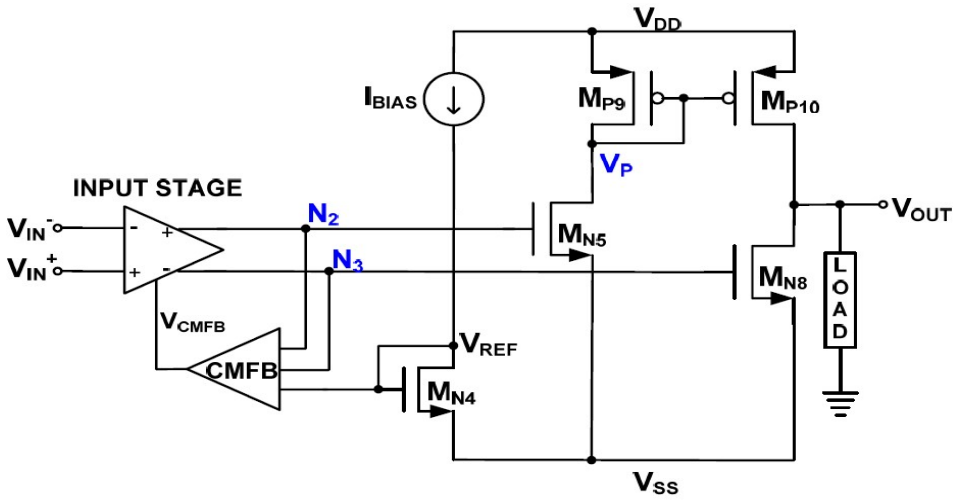


Figure 2.5: The output stage along with input stage and CMFB block diagram

The output stage used in this op amp is based on the circuit shown in Figure 2.5 along with its biasing section and are presentation of the input stage. This circuit topology is simple and provides capability for rail-to-rail output swing, good current drive and low power dissipation while using relatively small sized transistors.

2.4 Analogue Design Trade-offs

As discussed, to design an amplifier, there are a lot of issues to be considered. Parameters that can be named are gain, speed, power dissipation and supply voltage, linearity, noise, maximum swing and input and output impedances. These parameters interact with each other and there are trade-offs when optimizing for each parameter. For example, designing to have better noise performance needs the minimum size of transistors to be used which

obviously has a conflict of interest as linearity optimization include enlarging devices. Another way to lower nonlinearity is to increase overdrive voltages of MOSFETs which will cause more power dissipation. *Figure 2.6* shows the tradeoffs between performance parameters of amplifier.

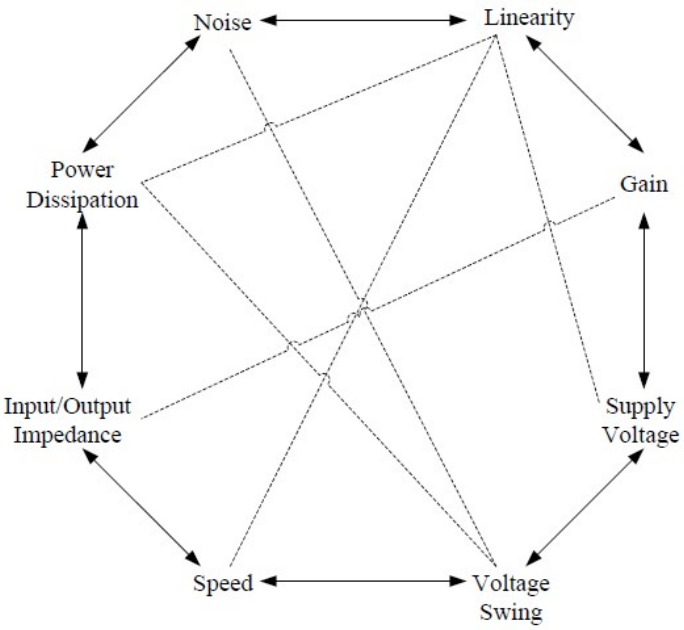


Figure 2.6: Analogue Design Octagon

2.5 OpAmps' Topologies

In this section two topologies of OpAmps are shown. First one is a telescopic topology and the second one is folded-cascode topology. Advantages and disadvantages of each topology are discussed. Then gain boosting and two-stage amplifiers are described. Adding a second stage and gain boosting of cascode devices help to achieve higher gain and also higher voltage swing in second case. At the end a comparison of performance between different topologies of amplifiers will be made.

2.5.1 Telescopic Topology

The first topology to be described here is a 1 stage telescopic amplifier. Telescopic topologies are used to achieve high gain. They increase the gain by boosting output impedance of the amplifier.

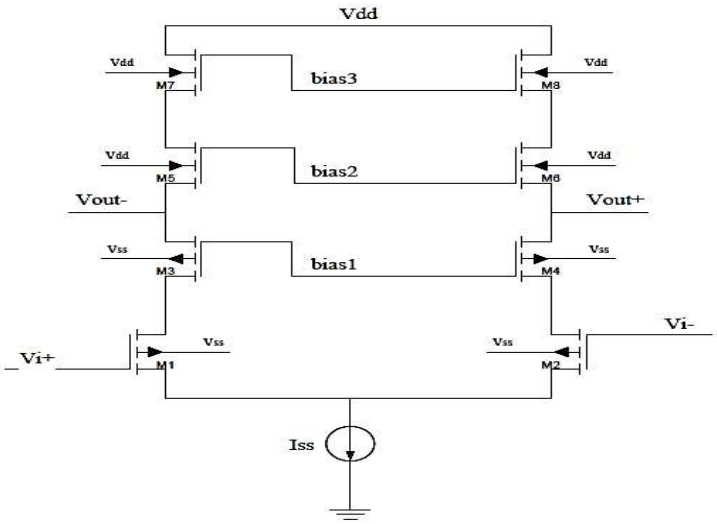


Figure 2.7: Telescopic Amplifier Topology

This structure is also called telescopic cascode configuration. Figure 3-6 shows a fully differential implementation of a cascode OpAmp. To achieve fully differential configuration current-source loads are used which at the same time will help with high gain requirement as well. It is informative to mention that diode-connected loads are used in single-ended output Operational Amplifiers' implementations and they exhibit a mirror pole introduced to the transfer function.

The output impedance seen from each single output node is equal to:

$$Rout = \left(\left[1 + (g_{m3} + g_{mb3})r_{o3}\right] \times r_{o1} + r_{o3}\right) \| \left(\left[1 + (g_{m5} + g_{mb5})r_{o5}\right] \times r_{o7} + r_{o5}\right) \quad (2.3)$$

As $G_m \sim g_{m1}$, then the gain can be calculated using Equation 2.4

$$A_v = G_m \times Rout \approx g_{m1} \times \left[(g_{m3} r_{o3} r_{o1}) \parallel (g_{m5} r_{o5} r_{o7}) \right] \quad (2.4)$$

One of the drawbacks of this implementation is the limited output swing. Each transistor cascaded on top of another one, adds an overdrive voltage to the headroom of output branch which will limit the output swing. Therefore, output swing of the fully differential implementation shown in *Figure 2.7* is obtained as:

$$Voltage - Swing = 2 \times \left[V_{dd} - \left(V_{ov1} + V_{ov3} + V_{ov5} + V_{ov7} + V_{Iss} \right) \right] \quad .5)$$

Where V_{Iss} isthe voltage drop over current source and $V_{ov}$is overdrive voltage of one transistor in the cascaded branch.

Another drawback is that extra poles are added to the small-signal transfer function of the OpAmp, exacerbating stability issue. When using this topology, one should be careful about minimum allowable input CM level and choosing bias voltages accordingly. For example, for bias1 we have:

$$CM - level_{\min} = V_{gs1} + V_{I_{ss}} \Rightarrow bias1 = V_{gs3} + V_{ov1} + V_{I_{ss}} \quad .6)$$

2.5.2 Folded-Cascode Topology

We saw that telescopic cascode OpAmps suffer from limited output swing. Folded-cascode OpAmps allow more swing at the output. Although, this topology consumes more power than telescopic topology due to its need for another current source (M3 and M4 act as a current source). This topology can be implemented either employing PMOS input devices or NMOS input devices. Each one has its advantages and disadvantages. In Figure 2.8 and Figure 2.9 two implementation of folded-cascode topology are shown:

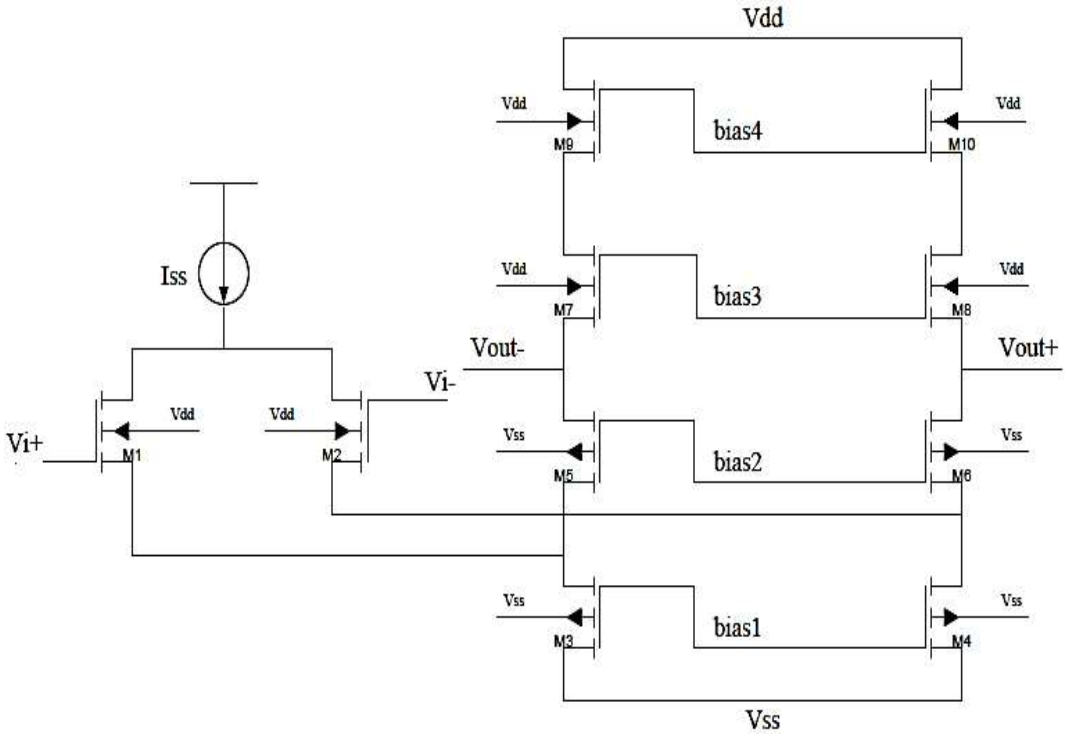


Figure 2.8: Folded-Cascode Implementation Using PMOS Input Devices

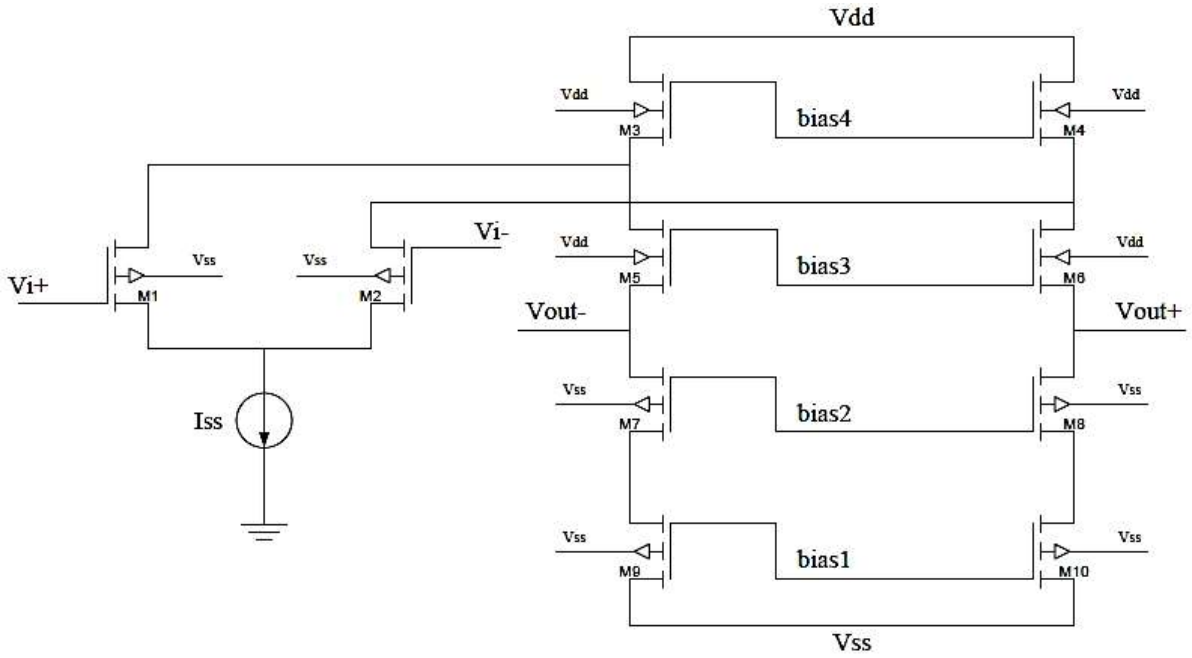


Figure 2.9: Folded-Cascode Implementation Using NMOS Input Devices

It can be seen that voltage swing in folded-cascode topology is higher than telescopic topology by one overdrive voltage across current source (V_{Iss}). So in the circuit of Figure 2.8:

$$Voltage - Swing = 2 \times \left[V_{dd} - \left(V_{ov3} + V_{ov5} + V_{ov7} + V_{ov9} \right) \right] \qquad (2.7)$$

Using the same approach as for telescopic OpAmp, the gain of folded-cascode topology can be obtained as:

$$\hat{Rout} = \left(\left[1 + (g_{m5} + g_{mb5}) r_{o5} \right] \times (r_{o3} \parallel r_{o1}) + r_{o5} \right) \parallel \left(\left[1 + (g_{m7} + g_{mb7}) r_{o7} \right] \times r_{o9} + r_{o7} \right) \qquad (2.8)$$

$$A_v = G_m \times Rout \approx g_{m1} \times \left[(g_{m5} r_{o5} (r_{o1} \parallel r_{o3}) \parallel (g_{m7} r_{o7} r_{o9}) \right] \qquad (2.9)$$

This gain is about 2-3 times less the gain of telescopic OpAmps. One reason is the lower transconductance of PMOS input devices compared to NMOS input devices. Another reason is appearing of in r_{o1}parallel with r_{o3}, which will reduce the output impedance of amplifier.

Another issue that should be kept in mind is that the pole in the source of cascode devices (M5 and M6 in Figure 2.8) is closer to the origin than that of telescopic OpAmp (M3 and M4 in Figure 2.7). In folded-cascode structure, capacitance in the mentioned node is made of intrinsic capacitances, other elements are from input and cascode devices which exist in both structures) than that of telescopic structure. This issue is exacerbated when using NMOS input devices. The reason lies within the need for larger PMOS transistors, as second current source, to carry both currents of input and cascode devices and obviously larger devices contribute more capacitance. Also lower transconductance of PMOS transistors, as cascode devices, increases the impedance of the node, which will help to bring pole to lower frequencies.

One of the important benefits of folded-cascode OpAmps is that their input CM level range is larger than that of telescopic OpAmps. Depending on the kind of input device, input CM level can be very close to one of the supply sources. In case of PMOS input devices, input CM level can be zero and having NMOS input device, OpAmp tolerate input CM level equal to Vdd. In general the choice of input device depends on the application. Whether gain is the target or CM level dictates the input device.

2.5.3 Gain-Boosting

In telescopic and folded-cascode topologies, increasing output impedance has been used as a means of increasing gain. In both, stacking more transistors in output branch as cascode devices helps to do so. What if there is a need for higher gain and larger output swing at the same time? Then, there would be no good outcome, inserting another level of transistors in the stack. The idea behind gain boosting is to increase the output impedance further more to achieve higher gain without adding more transistors to the output branch and reducing the swing as a result. In this approach, the cascode device is placed in a current- voltage feedback using an amplifier. Assuming telescopic OpAmp, both NMOS cascode devices in signal path and the PMOS cascode devices in the load current source can be used for gain boosting. In Figure 2.10 cascode transistors M3-M6 are placed in the feedback loop:

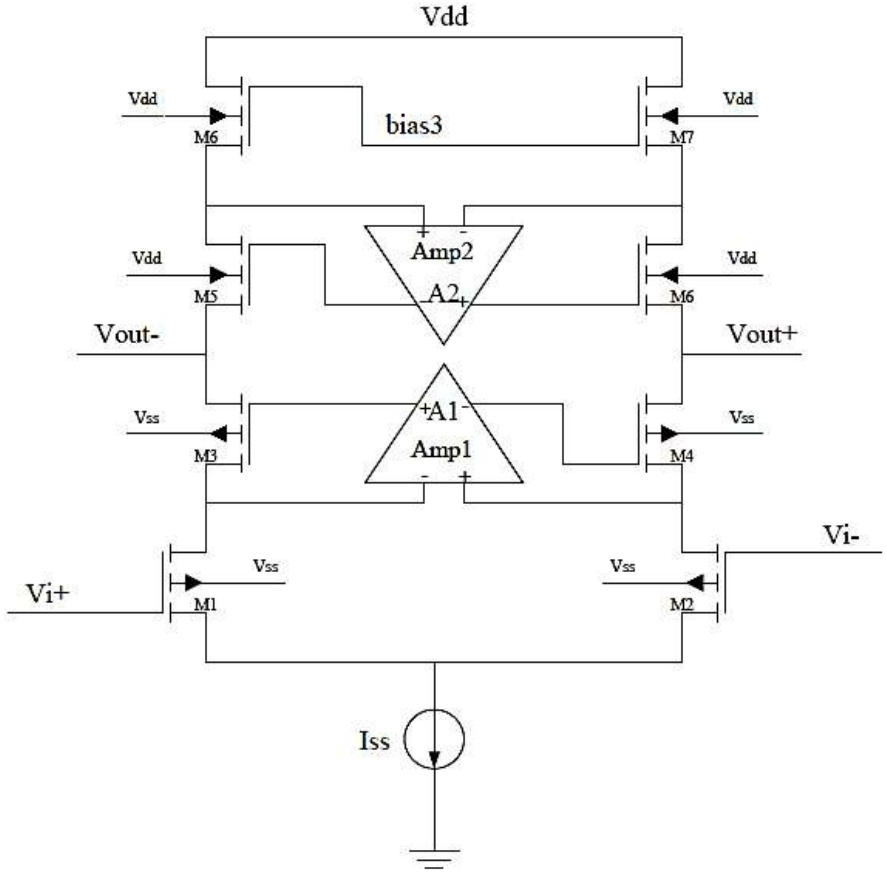


Figure 2.10: Gain Boosting Applied to Telescopic OpAmp Topology

The output impedance, using gain boosting technique, is obtained from parallel calculation of impedances seen by looking into drain of cascode devices, as before, but this time multiplied by the gain of auxiliary amplifiers A_1 and A_2.

$$Rout = \left(\left[1+(g_{m3}+g_{mb3})r_{o3}A_1\right]\times r_{o1}+r_{o3}\right) \| \left(\left[1+(g_{m5}+g_{mb5})r_{o5}A_2\right]\times r_{o7}+r_{o5}\right) \quad (2.10)$$

As $G_m \sim g_{m1}$, then the gain can be calculated:

$$A_v = G_m \times Rout \approx g_{m1} \times \left[(A_1 g_{m3} r_{o3} r_{o1}) \| (A_2 g_{m5} r_{o5} r_{o7})\right] \quad (2.11)$$

So, the gain is enhanced by increasing output impedance. The auxiliary amplifier can have any topology from a simple CS amplifier to fully differential folded-cascode topology. The sensing transistor at the input of these amplifiers should be chosen, such that they suit the CM level of the voltage being sensed (source of cascode devices). For example in Figure 2.10, if the Amp1 is a fully differential folded-cascode, the input devices should be PMOS as they can tolerate almost zero input CM level and the source voltage of M3 + M4 will become as low as $V_{ov1} + V_{Iss}$. Similarly, NMOS input devices are more suitable to be used in Amp2 as they will sense input CM level close to Vdd.

An important issue to remember is that, although the OpAmp is still a 1-stage amplifier, the poles in auxiliary amplifier will affect the transfer function. The effect wouldn't be very dramatic as the path is not the feed-forward path where most of the signal will flow through it. Nevertheless, one should be careful with stability around the extra loops created by gain boosting as well as stability around the main loop, placing the amplifier in closed loop configuration, when designing the circuit.

2.5.4 Two-Stage OpAmps

Two-stage OpAmps are used for their ability to provide more gain and swing. Basically, the second stage provides about 5-15 dB gain, which is not very high. But the higher output swing provided by the second stage is crucial to some applications, especially with lower supply voltages in today's technologies. So, the second stage is a simple amplifier like a CS stage, as shown in Figure 2.11below:

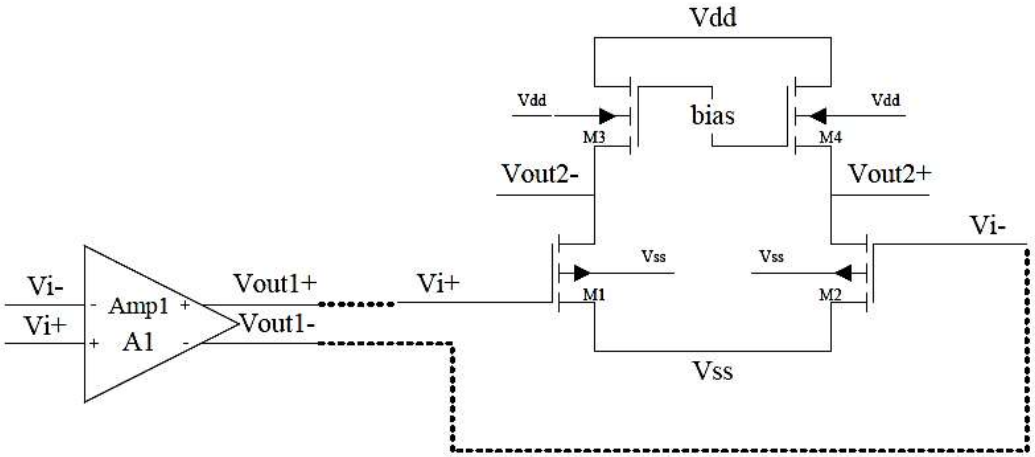


Figure 2.11: Two- Stage OpAmp

The second stage's gain is multiplied by the gain of the first stage:

$$A_{v-total} = A_{v1} \times A_{v2} = A_{v1} \times \left[g_{m1} (r_{o1} \parallel r_{o3}) \right] \quad 2.12)$$

The second stage's swing is much larger than say a telescopic output swing:

$$Voltage - Swing = 2 \times \left[V_{dd} - (V_{ov1} + V_{ov3}) \right] \quad (2.13)$$

The output stage's current should be high for the sake of speed, but, not that high to damage MOSFET devices or produce too much thermal noise. Obviously power dissipation should be kept under control too.

2.5.5 Comparison between Different Topologies of OpAmps

In this section, we sum up properties of different amplifier topologies that have been discussed in previous sections.

Telescopic OpAmps have high speed as the input device's current flows directly into output impedance, but they suffer from limited output swing. This topology is simple and

there is only one current source in it, so they dissipate power less than other topologies. Folded-cascode OpAmps stand next in the line. Compared to the telescopic topology they have less gain and speed and dissipate more power. But they have found their place in a wide range of applications due to their larger output swing and their extended input CM level range. Gain boosting and adding second stage is two powerful design schemes to obtain higher gain and in second case higher swing as well. As the level of the complexity of the circuit goes up, power consumption increases.

Bellow in Table 2.2 all properties of different topologies have been compared with each other:

Table 2.2: Comparison between Performances of Different OpAmp Topologies

	Gain	Output Swing	Speed	Power Consumption	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Gain Boosted	High	Medium	Medium	High	Medium
Two-Stage	High	Highest	Low	Medium	Low

In this work, a two-stage gain boosted amplifier is designed to achieve high DC-gain and output swing. The price to be paid is high power consumption which is not avoidable when a high performance amplifier is needed.

CHAPTER 3

COMPENSATED OP-AMP DESIGN FOR HIGH PSRR

In this chapter requirements of an OpAmp to be employed in a 12-bit pipelined ADC are discussed and calculated. After that the designed OpAmp and its performance metrics are shown. ADC structure and the use of designed OpAmp in the ADC will be described in next chapter.

3.1 OpAmp Requirements

For an OpAmp-based design of a high resolution and high speed pipelined ADC, there are high requirements for the OpAmp design to be satisfied. These two definition "high resolution" and "high speed" for an ADC adds a great deal of challenge on the OpAmp design to achieve the required performance regarding DC-gain, Bandwidth, noise, stability, speed and swing. All of which should be achieved under critical conditions of decreased supply voltages and intrinsic gain of today's CMOS technology. The down sized transistors of new coming technologies also have higher leakage and lower output resistance. They are faster switches as a result of the reduced parasitic capacitances (due to reduced transistor dimensions). Because of the higher number of transistors in smaller area, heat production is another problem of scaling in new technologies which will cause slower operation and reduced reliability and lifetime of the transistors. These transistors are also more prone to process variation. All of these characteristics of new scaled down technologies add more error to the Op-Amp's transfer function, making it harder to satisfy the stringent requirements on the OpAmp.

OpAmps are the basic building block of an ADC and other analog circuits, which determine the speed and accuracy of the ADC. They introduce gain error and nonlinearity which should be minimized in design process or compensated for by digital correction

circuitry. They are also the most power hungry part of the ADC and dissipate almost 60-80% of the total power. There are a few techniques to reduce OpAmps power consumption, like using class AB amplifiers which only consumes dynamic current, OpAmp sharing and OpAmp current reuse.

As discussed in Chapter 1 and 2, the OpAmp is used in the MDAC structure of the pipelined ADC. The OpAmp is placed in a negative feedback with amplification factor of 4. Now it is time to see what the requirement specification for this OpAmp is. Here we discuss DC-gain, Gain-Bandwidth (GBW), Slew-Rate (SR) and Noise.

- DC Gain
- GBW (unity gain frequency)
- Slew Rate
- Power Dissipation
- Supply Rejection (PSRR)
- Input Common Mode range (ICMR)

3.2 Design Challenges

A good understanding of the operation of MOS devices and op amp circuits when subjected to temperature variation is essential in designing an op amp to function at extreme temperatures. This section briefly discusses the behavior of MOSFET devices and its effect on op amp circuits at extreme temperature conditions.

3.2.1 Low Temperature (LT) behavior

The operation of semiconductor devices at cryogenic temperatures has been studied extensively for the past 3 decades because of the possibility of providing significant performance improvement at low temperature. Some of the notable advantages offered by low temperature operation include steeper subthreshold slope, substantial increase in

carrier mobility and saturation velocity, higher transconductance, reduced thermal noise, increased thermal conductivity, improved reliability through latch-up immunity, decrease in leakage current, and reduction of thermally activated failure processes. Operation at low temperature is challenged by the increase in threshold voltage, increased susceptibility to hot carrier degradation effects and impurity carrier freeze-out resulting in kink phenomenon and transient behavior of drain current at cryogenic temperatures.

3.2.2 High Temperature (HT) behavior

Study of high temperature electronics is mainly driven by industrial applications in geothermal sensors, space exploration and aircraft/automobile engine monitors. The limitations of HT operation are primarily due to lowering of mobility and thus a reduction in transconductance, increase in leakage currents, latch-up and reduced reliability of the oxide layer, metal interconnects and packaging. The parameters that are altered due to temperature variation have a major influence on device performance. These parameters are discussed here.

Threshold Voltage variation

In a standard expression for MOSFET threshold voltage, where φ is the Fermi potential, φ_s is metal-semiconductor work function difference, Q_{SS} is the extrinsic charge due to surface states, interface energy states, oxide traps etc., C_{OX} is the gate oxide capacitance, N_{SUB} is the substrate doping concentration, $_{Si}$ ε is the dielectric concentration of silicon, q is the electron charge. N_{SUB}, φs, Q_{SS}, C_{OX} are independent of temperature and the Fermi potential.

Which is dependent on temperature. With a reduction in temperature, the intrinsic carrier concentration, n_i, reduces and the Fermi potential, φ, increases, hence the threshold voltage increases at LT. In analog circuits the increase in V_{TH} at LT reduces the dynamic range of the circuit. Thus in an op amp, the ICMR would be reduced. For the CMOS

fabrication process used here, the V_{TH} of NMOS and PMOS devices vary approximately 200 mV across the temperature range of −180 °C to 125 °C

3.2.3 Mobility Variations

The carrier mobility variation across temperature presents a major constraint on circuits operating across extreme temperature ranges. At LT mobility may increase by a factor of 4 to 6, while at HT mobility decreases. The factors controlling mobility would help in understanding this temperature dependence. The carrier mobility μ is controlled by various scattering mechanisms like lattice scattering, ionized impurity scattering and vertical field dependent surface scattering. These mechanisms, and thus μ are a function of applied electric field, temperature, channel impurity concentration and the oxide layer thickness. At room temperature, for small gate voltages, surface scattering is relatively unimportant, so the surface mobility can approach bulk mobility. As gate voltage increases, inversion layer carriers are subjected to increased electric field and are pushed toward the surface, causing surface scattering to become more significant and lowers mobility. As temperature is lowered to near liquid nitrogen temperature (LNT) of about 77K, the reduction in the lattice vibration makes lattice scattering less significant. Therefore, mobility increases with reduction in temperature. The extent of this enhancement depends on other factors influencing mobility. For instance, in transistors with light doping near the surface, surface scattering effects dominate and mobility depends strongly on vertical field applied. For such devices, the enhancement in mobility at LNT over 27 °C is large for low vertical fields and less for higher fields. Also, devices built in wells are expected to have lower mobility at all temperatures and less μ enhancement since ionized impurity scattering, which is independent of the magnitude of vertical field, is significant at all temperatures.

The transconductance, g_m, for inversion-mode MOSFETs is proportional to the drift velocity in the channel and thus to the carrier mobility. Therefore, the variations in μ across temperature affect the transconductance and thus the gain and bandwidth of circuits.

3.2.4 Noise

The chief sources of noise in MOSFET devices are thermal noise and flicker noise. Thermal noise is due to the effective resistance of the channel and is directly dependent on the temperature of operation. The thermal noise can be represented as an input-referred PSD.

Thus, at LT the thermal noise can be significantly reduced, while at HT thermal noise increases and thereby affects the dynamic range of circuits. Flicker noise source is attributed to trapping levels along the Si-SiO_2 interface in the channel. This noise is larger than thermal noise for frequencies below 1 to 10 KHz for most bias conditions and device geometries.

At very LT, the increase in gate injection current, due to hot-carrier effects, results in an increase in oxide trapped charge and so flicker noise may actually increases lightly. Hence for low frequency applications where flicker noise is dominant, the noise might not always reduce with a decrease in temperature. At HT there is an increase in the thermal as well as the flicker noise.

3.2.5 Subthreshold Operation

In switching circuits, the variation of drain current with gate voltage in the subthreshold region is important in order to maintain the off current and control the switching characteristics.

Let C_{ox} is the gate-oxide capacitance, C_{si} is the silicon capacitance at the source boundary, and C_{ss} is the capacitance associated with charging and discharging interface traps. The capacitances do not vary much with temperature, but the subthreshold slope S depends on the temperature. It has been shown in various articles that the typical values of S improved by a factor of 4at 77 K when compared to the room temperature value. Thus at

LT, the subthreshold slope is steep requiring a small voltage change to cause a large change in current (e.g.,“off” to “on”).

3.2.6 Reliability

The reliability of CMOS devices is a strong function of operating voltage and temperature. At LT, the mechanisms that cause failure such as latch up, electro-migration, oxide breakdown are reduced, thus improving the reliability. But at HT, these failure mechanisms dominate and thereby affect the reliable operation of devices.

Latch-up is due to the presence of parasitic bipolar transistor structures formed within the process cross section. The parameters that control latch-up such as holding current, holding voltage, and trigger current depend on the current gain β of the parasitic transistors and on the forward base-emitter voltages and are therefore dependent on temperature. Latch-up can be triggered by transient current flow and would cause failure by the positive feedback action in the parasitic BJTs. At LT the gain of BJTs is very low such that the total gain in the parasitic BJTs is less than unity and thus latch-up is suppressed. But at HT the increase in β enhances the likelihood of latch-up to occur.

Electro-migration, caused by the creation of metal voids and shorts in metal interconnects due to the movement of metal atoms at high current densities, has a thermal activation process. So at LT electro-migration is significantly reduced, but at HT electro-migration reduces reliable circuit operation.

Hot carrier degradation effects: When high electric field is applied, the carriers gain high kinetic energy and may be injected into the gate oxide and become trapped there. This changes the MOSFET’s threshold voltage and transconductance. At LT the reduced lattice scattering due to lattice vibrations results in a large fraction of carriers reaching the gate and a high susceptibility to hot carrier degradation. At -180 °C(77 K), there is an increase in these effects. This augmentation is not due to the enhanced trapping in oxide, but due to

increased influence of trapped charge on device operation[10]. The degradation can be controlled by operating the devices with lower voltages and thus placing a design constraint on the gate voltage.

3.2.7 Carrier Freeze-out

At and above room temperature, essentially all the impurity atoms are thermally ionized and the concentration of mobile carriers is equal to the dopant concentration. As temperature decreases, the Fermi level approaches the valence band causing the mobile carriers to begin to freeze-out on the impurities and a corresponding decrease in electrical conductivity is observed. The carrier freeze-out situation at the semiconductor surface under the gate is different than that in the bulk due to band bending. The electric field of the channel interface depletion region sweeps out any mobile carriers and maintains complete ionization even at low temperatures. Approaching LNT carriers in the bulk begin to freeze-out, but there is essentially no effect on the ionized impurity concentration in the depletion region. At strong freeze-out conditions of temperature below 30K, kink effect and transient phenomenon on I-V characteristics are observed.

Kink effect: At LT when impurity freeze-out occurs, the MOS devices in saturation region experience kink effect that is attributed to self-polarization of the substrate due to the flow of majority carriers from body to source. The impurity freeze out in the bulk leads to a strong increase of the back resistance which prevents the collection of drain impact ionization current through the body contacts. This results in a self-biasing of the body and the source-body junction becomes forward biased. This causes a change in the threshold voltage and produces leveling of the drain current in saturation resulting in a kink in the I-V characteristics.

Transient effects: At LT operation when freeze-out occurs, when the gate voltage is increased from accumulation to inversion mode of operation, the drain current rises very rapidly to a value larger than the steady state value and then relaxes to the equilibrium

steady state value. This is attributed to the slow formation of the depletion region that is dependent on temperature. As soon as the gate voltage is stepped up, the space charge induced is mostly inversion charge since the dopant atoms have not hadthe time to emit charge and get ionized. However as time progresses, the dopant atoms get ionized and depletion region forms. As depletion region grows to its equilibrium level, the inversion charge decays to its steady state value. Since I_D is proportional to inversion charge, I_D exhibits the same type of transient behavior.

3.2.8 Leakage Current

With increasing operating temperature, there is an exponential increase in the leakage currents flowing across reverse-biased *p-n* junctions such as the drain/source and substrate junctions in a MOSFET. These drain leakage currents are amplified by parasitic bipolar transistors which also cause latch-up. This amplification results in leakage currents that are much higher than the original diffusion leakage currents caused by the *pn* junction of the drain-substrate bulk diode. At 250 °C, the leakage current increases by a factor of 4 than at 25 °C and becomes comparable to the drain current of the device. These large leakage currents cause drifts in the operating points of the devices and the circuit and may also result in latch-up. Thus, circuit operation at high temperatures is affected by leakage currents and proper design is required to compensate for the leakage currents.

3.2.9 Effect on Op amp circuits

Following the study of temperature effects on MOSFETs, a brief discussion on the temperature dependence of op amp parameters is presented here using a simple two stage CMOS op amp. The dependence of V_{TH} and μ*(mobility)*on temperature has a major impact on the performance of the op amp. The dynamic range of the op amp, which is impacted by offset voltage, noise and ICMR, is affected by variation in temperature. The change in threshold voltage causes bias point shifts and may thereby change the systematic offset voltage of the circuit. The noise contributed by the op amp also varies with a positive

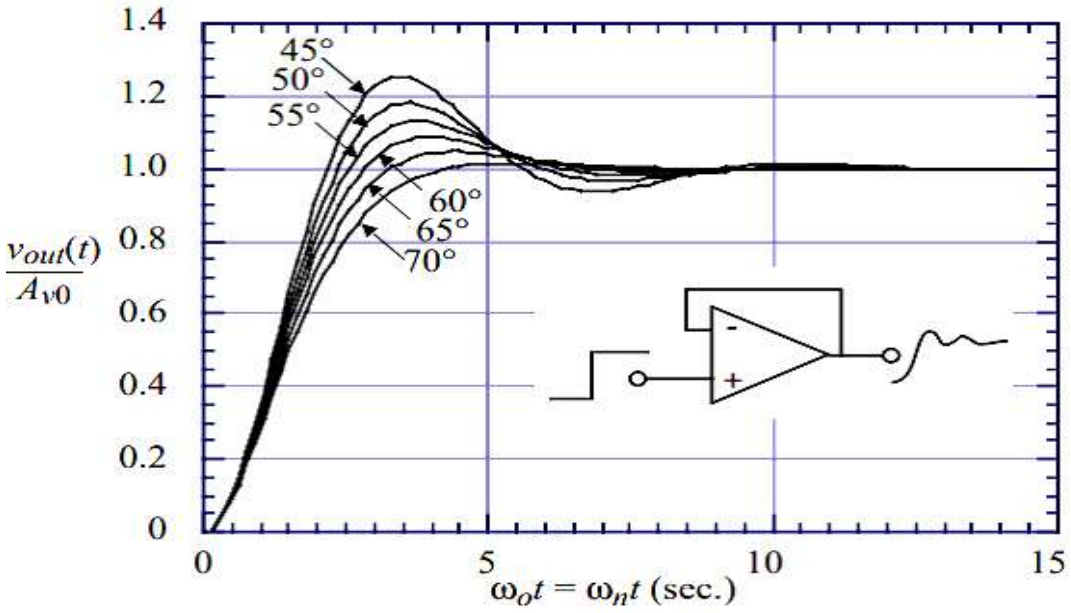
temperature coefficient. The input common-mode range (ICMR) is the input voltage range that is available for linear operation.

The temperature dependence of the threshold voltage affects the ICMR. At LT, the increase in threshold voltage lowers the ICMR. In order to increase the available ICMR, the $V_{DS,sat}$ of the device could be maintained at a minimum level of about 100mV for moderate inversion saturation operation. For strong inversion saturation, $V_{DS,sat}$ can be lowered by reducing current I_D, increasing width, and by decreasing length. Any change in these device parameters would in turn affect the performance. For instance, reducing I_D would reduce the cut-off frequency of the op amp. With decreasing lengths, the cut-off frequency increases due to a reduction in the gate capacitance, but the offset voltage and flicker noise increase. Also, decreasing L reduces the output impedance and thus the gain decreases. As width is increased, the bandwidth decreases because of the increase in the drain/source capacitance. So, there already exist many tradeoffs in designing an op amp for a specific temperature and extending the operability to extreme temperatures only adds more constraints to the design. Considering the effect of mobility variations across temperature, the transconductance also changes with a negative temperature coefficient. This leads to a change in the gain A_{OL}, bandwidth and phase margin across temperature. When operated at HT, g_m decreases and so gain falls along with the bandwidth. To circumvent this problem, the current reference that is used to provide the bias current for the opamp could be designed to enhance robustness of the circuit across temperature. One method is to provide a constant-g_m bias circuit which stabilizes the small-signal performance. Providing a constant-g_m does not imply a constant current and thus results in changes in the large-signal response, such as the slew rate, across temperature. Another method is to provide a constant current across temperature. This constant current minimizes the variation of large-signal performance of the circuit, but at the expense of small-signal performance.

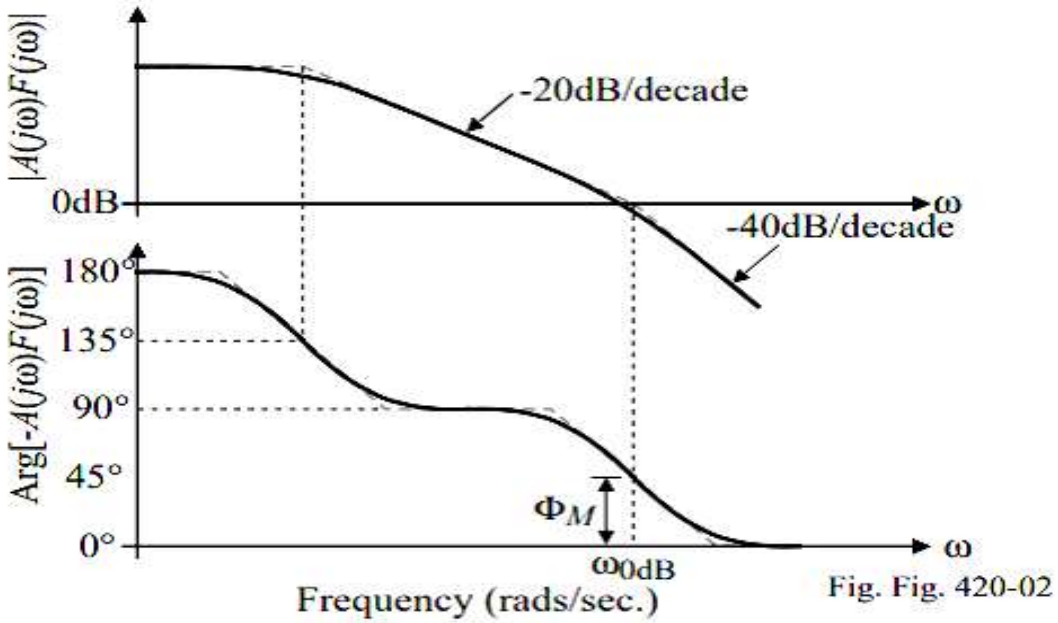
Therefore, proper design procedure is required to minimize the parameter variations across temperature. The following chapter deals with the design procedure used to build a robust circuit that operates well across temperature.

3.3 Two stage Miller Compensated op-Amp Design

CMOS operational amplifiers are one of the most fundamental, versatile and integral building blocks of many analog and mixed-signal circuits and system. They are used in a wide range of applications such as comparators, differentiators, dc bias applications and many other applications. IC designers tend to design systems with a single dominated pole behavior because these are easily analyzed and can tolerate negative feedback without stability issues. As a result, single stage operational amplifiers have been preferred for their stable frequency response. However, CMOS technology has been constantly scaling down establishing some challenges when designing operational amplifiers and others integrated circuits. Additionally, the power supply voltage has also been reduced, causing techniques like cascading of transistors more difficult to implement. The new scaled processes enable faster speeds, but lower open loop gains and the reduction in voltage does not allow for cascading multiple stages to achieve higher gains. Therefore, alternative architectures must be implemented to overcome the drawback of single stage amplifiers. Multiple stage amplifiers can be implemented to achieve higher gains circuit designs regardless of the limitations of the power supply voltage and other performance aspects that affect single stage amplifiers. However, multiple stage amplifiers are generally complex to compensate. Two-stage operational amplifiers are the most common used multistage amplifier because it can provide high gain and high output swing. However, an uncompensated two-stage operational amplifier has a two-pole transfer function, and these are located below the unity gain frequency. Therefore, a frequency compensation circuitry must be implemented to ensure stability *(Figure 3.1)*. It is difficult to design a system with a truly single pole behavior; nevertheless, this desire behavior can be approximate over a frequency range that falls under the desire design specifications.



(a)



(b)

Figure 3.1: Stability problem on an two stage amplifier and how it is important for the step response (a) transient response interpretation (b) Bode plot interpretation [1, 3]

Operational amplifiers operated on a close-loop with a negative-feedback system are susceptible to oscillation. The measurement of stability of an operational amplifier is the phase angle at unity open-loop gain and this is given by [1]:

$$PhaseMargin = \Phi_M = [-A(j\omega_{0,dB})F(j\omega_{0,dB})] = Arg[L(j\omega_{0,dB})] \quad (3.1)$$

Where the negative feedback is illustrated as follow:

$$(s) = -A(s)F(s) : Open-LoopGain \quad (3.2)$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)}{1+A(s)F(s)} : Closed-Loop\ Gain \quad (3.3)$$

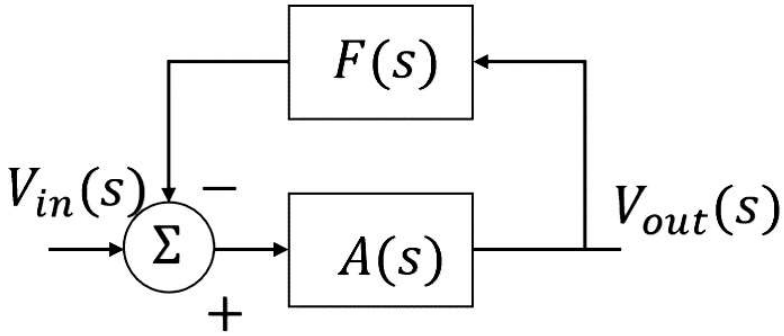


Figure 3.2: Block Diagram of feedback configuration

Due to the parasitic components on the amplifier, in addition to attenuation there is a phase shift between input and output, and oscillations will happen when the phase shift (phase margin) exceeds 180 degrees. A phase margin of 180 degrees turns negative feedback into positive feedback causing the amplifier to oscillate. As a result, the more stages an amplifier has, the more unstable its behavior is, requiring more complex compensation methods. As a rule of thumb, a 45 degree or greater is a phase margin that will yield good stability and less overshoot [1, 3]. Furthermore, as shown on *figure 3.1 (a),* stability is

important in order to have a good step response of the amplifier. The desired behavior of an amplifier is to reach its final value quickly; therefore, the amplifier must be stable and have a phase margin at least greater than 45 degrees.

3.4 Design Procedure

This section presents a design procedure for a basic miller compensated two stage CMOS op amp (figure 3.3) with basic op amp equations.

The following equations are the MOSFET, strong inversion, square law equations:

$$\text{Drain current} \quad I_D = \beta V_{OV}{}^2 = \frac{\mu_{n,p} C_{ox}}{2} * \left(\frac{W}{L}\right) * V_{OV}{}^2$$

$$\text{where} \quad \beta = \frac{\mu_{n,p} C_{ox}}{2} * \left(\frac{W}{L}\right)$$

$$\text{Drain current} \quad I_D = \beta V_{OV}{}^2 = \frac{\mu_{n,p} C_{ox}}{2} * \left(\frac{W}{L}\right) * V_{OV}{}^2$$

$$\text{where} \quad \beta = \frac{\mu_{n,p} C_{ox}}{2} * \left(\frac{W}{L}\right)$$

$$\text{Aspect ratio} \quad \frac{W}{L} = \frac{2I_D}{\mu_{n,p} C_{ox} * V_{OV}{}^2}$$

$$\text{Transconductance,} \quad g_m = \sqrt{2 * \mu_{n,p} C_{OX} * \left(\frac{W}{L}\right) * I_D}$$

$$g_m = \frac{2 * I_D}{V_{OV}}$$

The following design consist of an NMOS differential amplifier with active load as the first stage follow by a PMOS common source amplifier as the second stage. A compensation capacitor is connected between the output of the second stage and the output of the first stage to obtained pole splitting and hence op-amp compensation.

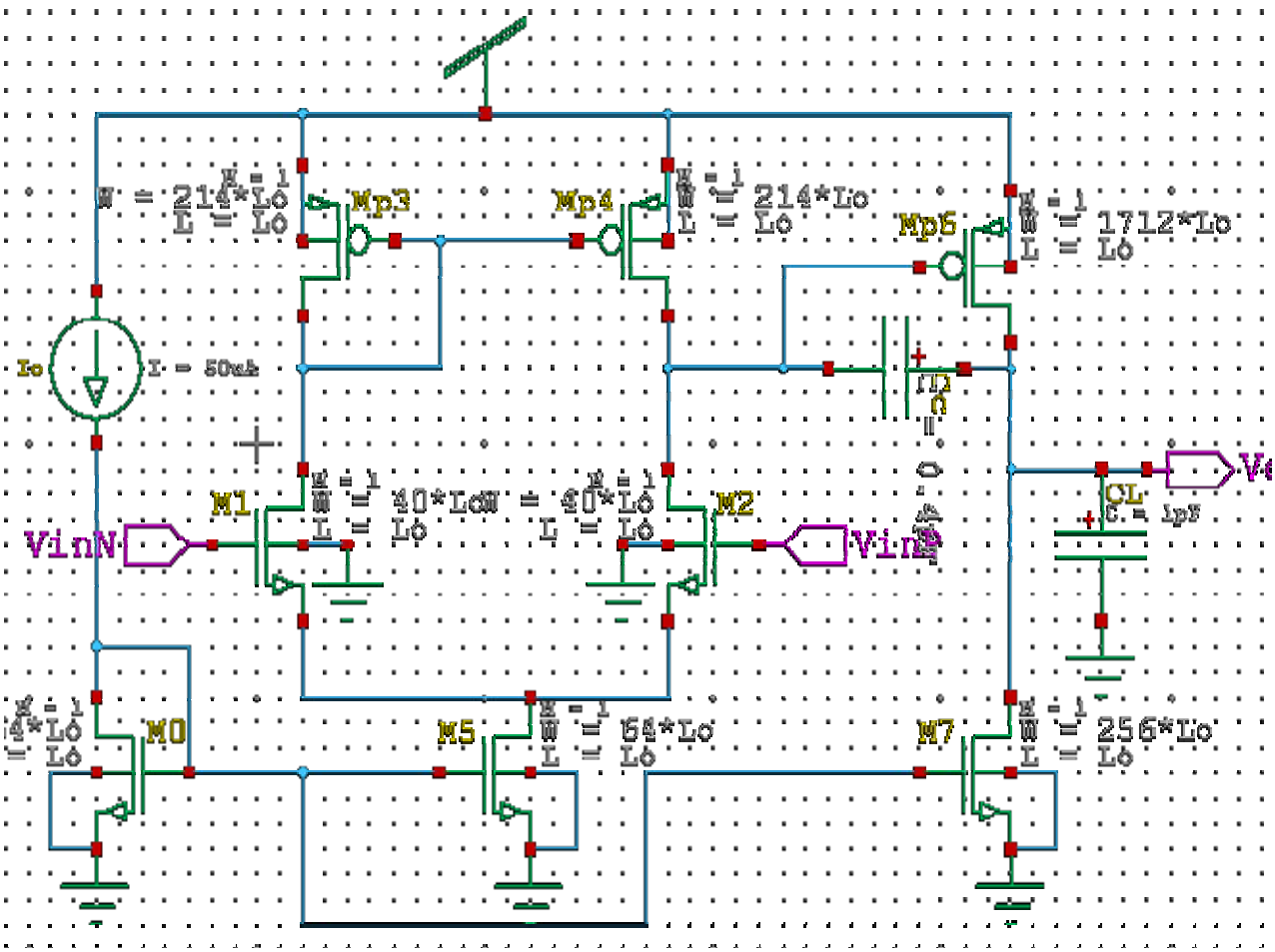


Figure 3.3: Miller compensated two stage operational amplifier (transistor level schematic in SPICE environment)

The following design consist of an NMOS differential amplifier with active load as the first stage follow by a PMOS common source amplifier as the second stage. A compensation capacitor is connected between the output of the second stage and the output of the first stage to obtained pole splitting and hence op-amp compensation.

The two-stage operation amplifier with Miller compensation achieved the desired specifications based on the sizing showed in figure 3.3. As shown below on the frequency

response of the operational amplifier, the system behaved as a single pole system before the unity gain frequency. This allows a better phase margin for the operational amplifier thus achieving better stability.

STEP 1: Design the compensation capacitor Cc in such a way that placing the pole P2 , 2.2 times higher than the Gain bandwidth product (GB) permitted a 600 phase margin. This results in the following requirement for the minimum value for Cc.

$$C_c > \frac{2.2}{10} * C_L$$
$$C_c > \frac{2.2}{10} * 10 * 10^{-12}$$
$$C_c > 2.2 * 10^{-12}$$

Choose C_c=2.3pF

STEP 2: The next step of the design is the estimation of the bias current. From the slew rate specification, we have

Slew rate (SR) = $\frac{I_{SS}}{C_c} = \frac{I_5}{C_c}$

Where I_{SS} (=I_5) is the tail current.

I5 = S. R ∗ Cc = 50 * 106 * 2.3 * 10−12= 115 μA

STEP 3: Assuming the GB established by the dominant node, we have

gm1 = GB * Cc = 2 * ∏ * f * Cc

gm1 = 120 * 106 * 2.3 * 10^{-12}

= 0.0017 = 1.7 m Ω^{-1}

$$\left(\frac{W}{L}\right)_{1,2} = \frac{(g_{m,1})^2}{K_n * I_5}$$

$$= \frac{(1.7 * 10^{-3})^2}{343.2 * 10^{-6} * 115 * 10^{-6}}$$

$$= 73.22$$

STEP 4: Design for W/L for M3 and M4 from the maximum input voltage specification.

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_5}{K_p * [V_{DD} - V_{in}(\max) - |V_{tp,3}|(\max) + V_{tn,1}(\min)]^2}$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{115 * 10^{-6}}{70.4 * 10^{-6}[1.65 - 1.3 - 0.42 + 0.42)]^2}$$

$$= 14$$

STEP 4: Design for W/L for M5 from the minimum input voltage specification.

$$V_{DS5} = V_{in}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{tn,1}(\max)$$

$$= -0.8 - (-1.65) - \sqrt{\frac{115 * 10^{-6}}{343.2 * 10^{-6} * \frac{73.22}{2}}} - 0.57$$

$$= 0.1867$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_5}{K_n C_{OX} * {V_{DS5}}^2} = \frac{2 * 115 * 10^{-6}}{343.2 * 10^{-6} * (0.1867)^2} = 19.22$$

STEP 6: Find gm6, gm4 to design W/L of M6

$$g_{m6} = 10 * g_{m1}$$

$$= 10 * 1.7 * 10^{-3}$$

$$= 17 \text{ m } \Omega^{-1}$$

$$g_{m3} = \sqrt{\frac{2*K_p*\left(\frac{W}{L}\right)_3*I_5}{2}}$$

$$= \sqrt{\frac{2*70.4*10^{-6}*14*115*10^{-6}}{2}}$$

$$= 0.337 \text{ m } \Omega^{-1}$$

Let $V_{SG,4} = V_{SG,6}$

Therefore, $\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 * \frac{g_{m,6}}{g_{m,4}}$

$$= 14 * \frac{17*10^{-3}}{0.337*10^{-3}}$$

$$= 706.23$$

STEP 7: Calculate I_6flowing through M6

$$I_6 = \frac{(g_{m,6})^2}{2 * K_p*\left(\frac{W}{L}\right)_6}$$

$$= \frac{(17*10^{-3})^2}{2*70.4*10^{-6}*706.23}$$

$$= 2.9 \text{ mA}$$

STEP 8: Design W/L for M7 to achieve the desired current ratios between I6 and I5

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5 * \frac{I_6}{I_5}$$

$$= 19.22 * \frac{2.9*10^{-3}}{115*10^{-6}}$$

$$= 484.67$$

STEP 9: Design W/L for M8 by relationship relating to load, compensation capacitors, and W/L of M6

$$\left(\frac{W}{L}\right)_8 = \frac{\left(\frac{W}{L}\right)_6}{1+\frac{C_L}{C_c}} = \frac{706.23}{1+\frac{10*\mathbf{10^{-12}}}{\mathbf{2.3*10^{-12}}}} = 132$$

This completes all the design parameter of the proposed Op-amp architecture in figure 3.3.

CHAPTER 4

DESIGN SIMULATIONS AND RESULTS

This chapter presents the simulation setups and results corresponding to the various mode of analyses, in order to validate the proposed performance of the amplifier. With the technological parameter extracted earlier, here comes step by step results' analyses of the design in 180 nm CMOS technology with 1.8 V power supply and 2 pF load capacitance.

4.1 Design Constraints

The miller compensated two stage op amp with robust biasing circuit is shown in Figure 2 as a topological adoption and *Figure 4.1* in the next section depicts the exact implementation of it in *180 nm CMOS* technology with *1.8 V* bias. It could be noticed from figure 2, that both the primary differential stage and the second common source gain stages are implemented in fundamental transconductance mode. This appears due to the fact that the transistor (*MOS*) based amplifiers fundamentally offer the transconductance gain rather than the voltage gains, hence an additional output buffer is required to convert the current mode to the voltage mode at the output with a high current driving capability [3]. As the major aim of the design presented in this paper is to achieve a high gain (*GBW*) along with high *PSRR*, the output buffer design is not a major concern (hence neglected in actual implementation). The non-idealities of the transcoductance amplifiers ($g_{m1}$and g_{m2}) are modelled by output resistance and capacitive effect at each output node of the amplifier. These output resistances basically account for the channel length modulation (*CLM*) effect of the small scale devices. The first of the two stages usually consists of high gain, differential amplifier (and the same is implemented here also). The common source amplifier as a second stage usually meets the expectation of the additional gain.

Practically the Op-amp is always used with negative feedback. Negative feedback is used to reduce the error at output and provide stability to the system. Bandwidth Improvement

with the help of feedback the dominant pole will be shifted as a result the bandwidth will increase. Without feedback, the distortions were arising due to harmonics as a result of which lots of energy were consumed in harmonics but with the help of feedback linearity is increased [3, 26, 27].

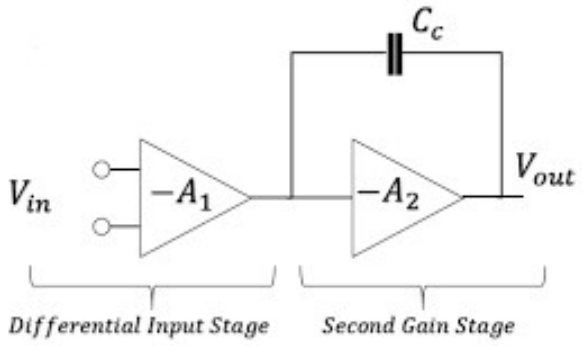


Figure 4.1: Two stage topology adopted, for miller compensating Op-Amp, in this work ($C_{cmp} \sim Cc$)

This second stage is included in op-amp architecture so that the higher gain can be obtained along with a larger swing. The gain improved in second stage is in the range of *5 to 15 dB [27, 28]*. The second stage is nothing but the Common source amplifier. Since it is common source, source of *MOS*-transistor is ground which is clearer from the figure 2 shown below.

The major features of the proposed Op-Amp are listed below:

a) *The differential amplifier used above is having two equal but opposite inputs and common output hence known as single ended amplifier.*

b) *This differential pair is identical and mirror image of each other, hence the current which is flowing through each of them will be same. If it is assumed that* $I_{(SS)}$ *is the*

current provided by the current source, then the current flowing through M_1 and M_2 will be I(SS)/2.

c) *From figure 2 and 7 of the next section, it is also clear that MOS transistor M_1 and M_2 are V to I (Voltage to current) converter. Since these two transistors are taking voltage at their input terminals and converting the energy into current.*

d) *Also MOS transistor M_3 and M_4 are I to V (Current to voltage converter).*

e) *Then again, the transistor M_7 will convert voltage obtained from M_4 into current.Finally, the MOS M_6 is provided to convert back that current provide by M_7 into voltage. Hence at the end we obtain output voltage as v(out). It should also keep in mind that if the Amplifier is driving the capacitive load then we completely neglect the output buffer stage.*

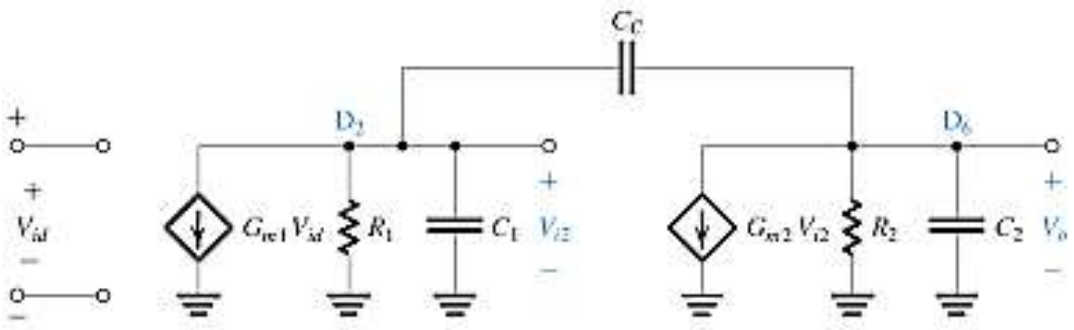


Figure 4.2: Simplified small-signal equivalent circuit of the amplifier of figure 2 describing the gain and effect of compensating capacitor

The biasing of the operational amplifier is achieved with four transistors. Transistors M_6 and M_7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string *(Figure 4.4 and 4.5)*. In this circuit proper biasing of other transistors in the circuit (M_1-M_5) is controlled by the node voltages. $M_5$is biased by the gate to source voltage (V_{GS}) set up by the V_{GS} of the current mirror load as are the transistors M_1

and M_2 as shown in above *figure 4.5*, and their equivalent diagram in figure 4. The designed and implemented in this project is a two-stage operational amplifier with an n-channel input pair. And op-amp uses a dual-polarity power supply $V_{dd}$and V_{ss} so the given ac signals can swing above and below ground. At the output the capacitance is to be connected as shown in *figure 4.2.* The design of two stage op-amp includes all the process parameters into account and which contribute in performance of overall gain of the system. High gain, bandwidth, and good power supply rejection ratio (*PSRR*) and common mode rejection ratio (*CMRR*) are some of the desired features of a good operational amplifier.

4.2 Estimated parameters

The Thevenin's equivalent of the Op-Amp has been shown in *Figure 4.3* below, displaying trendy op amp notations. It amplifies the voltage difference, $V_d = V_p - V_n$, (or $V_+ - V_-$ here), at the entry port and produces an output voltage, Vout, at the output port. The perfect op amp version was derived to simplify circuit calculations and is typically utilized by engineers in first order approximation calculations. The most idealized version makes 3 simplifying assumptions:

- *Open Loop Gain* $Av = \infty$ *(here* $G = \infty$*)*
- *Input Resistance* $Rin = \infty$
- *Output Resistance* $Rout = 0$

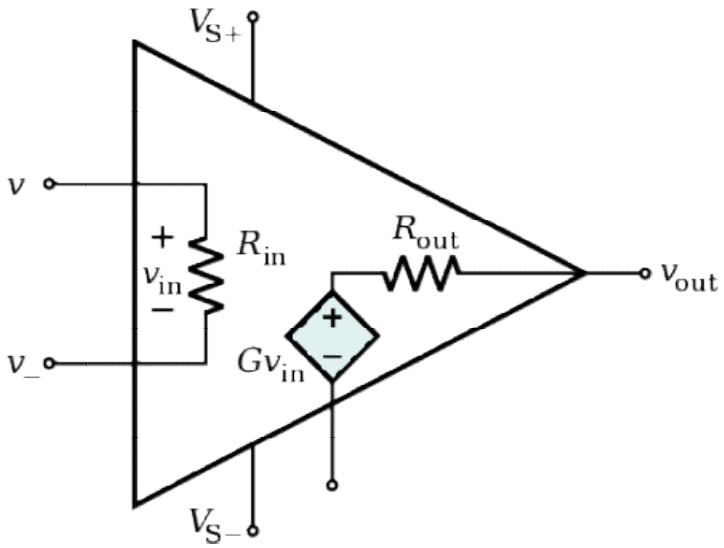


Figure 4.3: Standard op amp notation (amplifier model)

These assumptions have been considered while developing the small signal model of the two stage high gain Op-Amp in *Figures 4.2 and 4.3*. Only the overall gain of the Op-Amp has been considered practical that is finite, hence the finite output resistances (R_1 and R_2) have been made accountable for this. Two stage operational amplifiers provide high gain and high output swing [18, 19, 20]. For low frequency applications the gain is one of the most critical parameters. Overall gain is given by:

Net DC gain of the Op-Amp*:* $A_V = A_{V1} * A_{V2}$***(targeted ≥70 dB)***

Where

A_{V1} *(gain of 1st stage op amp)* $= gm_1 (rds_2 || rds_4)$

A_{V2} *(gain of 2nd stage op amp)* $= gm_7 (rds_6 || rds_7)$

Maximum Output swing = $V_{DD} - |V_{OD5}|$

Minimum Output swing = $|V_{OD6}|$

$$gm = \sqrt{(\mu n * Cox(W/L) * 2Id}$$

Temperature coeff. $= [(V_{max}-V_{min}) / (\Delta\ T^*$ *Voltage at 27'C)]* $*10^6$

$R_0=1/\ 2\pi r_0 C_0$

$ICMR_{max} = V_{DD}-V_{OD}+V_{t1}$ ***(targeted 1.6 V)***

$ICMR_{min} = V_{gs1}+V_{OD}$ ***(targeted 0.6 V)***

Slew-rate $(V/\mu s) = I_{max}/C = I_{out}/Cc$ ***(targeted 20 V/µs)***

As the very fisrt step for any Analog CMOS design startup is to finalize the technological node parameters (μ, *Cox and* V_T), a circuital arrangement is estabilished in order to achieve the same (*Figure 4.4*).

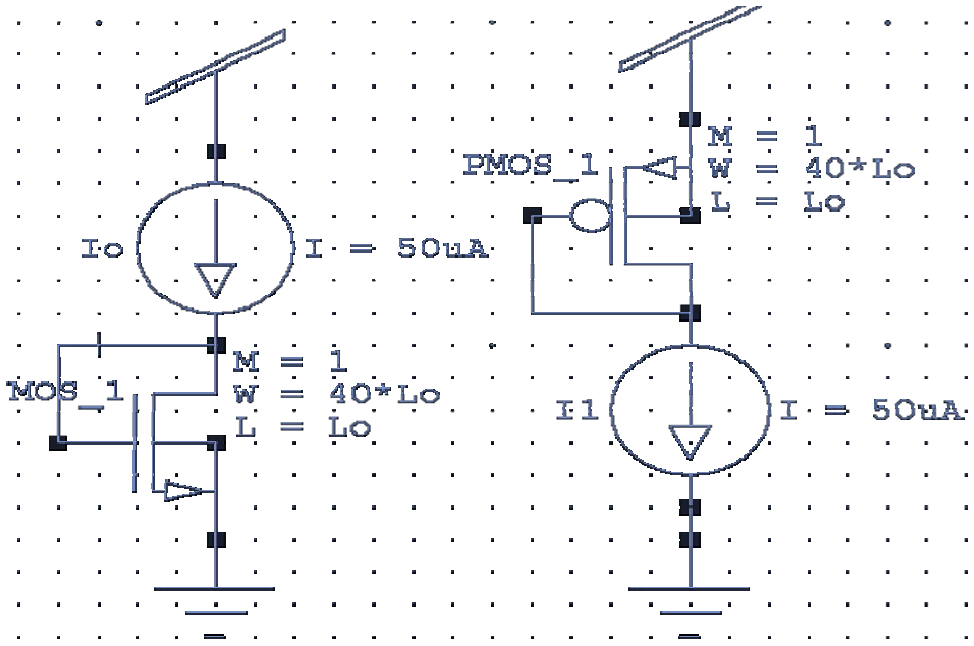


Figure 4.4: Experimental setup for technological parameter extraction

The *DC* simulation setup of *figure 4.4* provides the transconductance factor value (μC_{ox}) in addition to the idea of threshold voltages of both *PMOS* and *NMOS* transistors. The values obtained are:

$\mu_p C_{ox} = 60\ \mu A/V^2$ *(for L= 500 nm)*

$\mu_n C_{ox} = 300\ \mu A/V^2$ *(for L= 500 nm)*

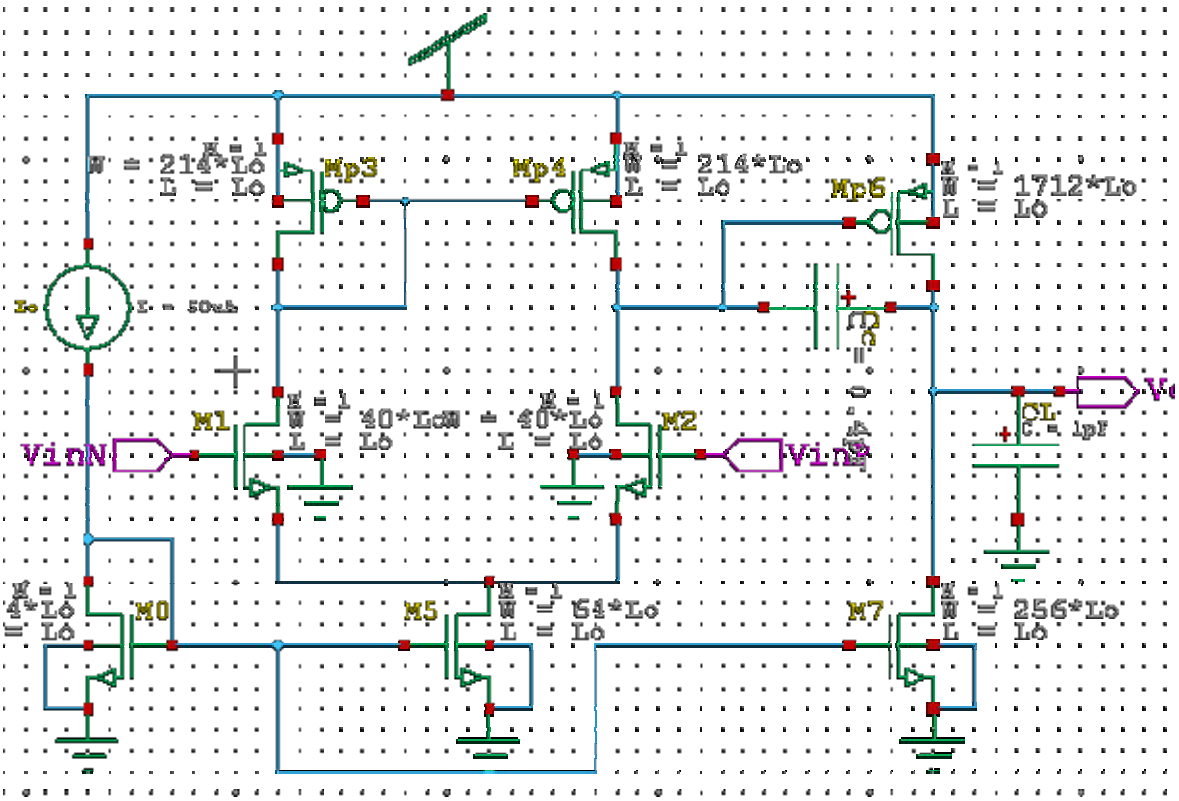


Figure 4.5: Miller compensated two stage operational amplifier (transistor level schematic in SPICE environment)

Now these values setup the starting design procedure of the transistor based schematic of an amplifier foer manual interpretation. The schematic detailing (*figure 4.5*) of the proposed op-amp design reveals the finer details about the circuit like biasing arrangement, mode of the transistors, amplifier topology and supply mode. As one can easily notice that the circuit implementation is the exact replica of the proposed two stage model of the design in *figure 4.2 and figure 4.3*.

Setup 1: Op-Amp Design and DC simulation

This is the very first simulation setup (*Figure 4.6*) for any amplifier topology in order to ensure the proper mode of the active transistors, with biasing arrangements and given power supply. The major job of this DC simulation here is to verify the common mode range operation and check the compliance of the design with targeted input common mode range (*ICMR)* in addition to the mode of the transistors.

- At $ICMR^{+} = 1.6\ V$: All Transistors in Saturation

(with $Gm = 543\ \mu S$ for M_1 and M_2), $P_D = 294\ \mu W$

- At $ICMR^{-} = 0.6\ V$: All Transistors in Saturation

(with $Gm = 483\ \mu S$ for M_1 and M_2), $P_D = 280\ \mu W$

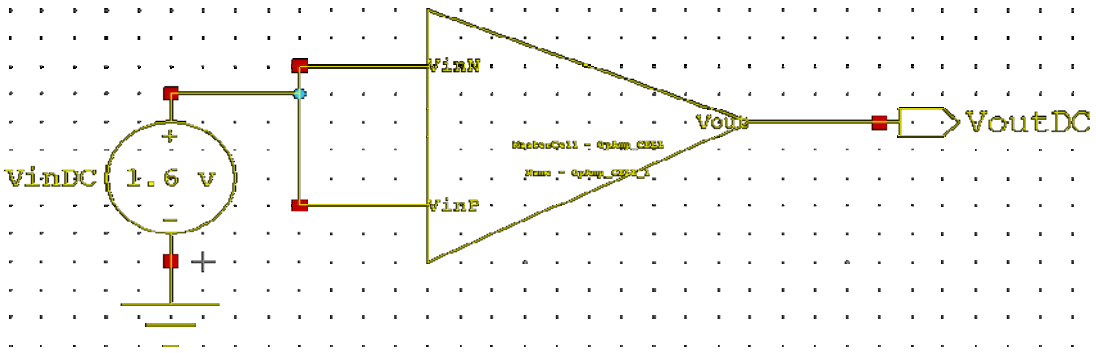


Figure 4.6: DC analysis validation for ICMR and Gm, Vin= 1.6 V (a similar setup is taken for Vin = 0.6 V)

Therefore, the transconductance gains of the active transistors (M_1 and M_2) remains $500\ \mu S$ approximately. The *DC* power dissipation has also been measured which comes out to be $290\ \mu W$, which is fairly the appreciable value for the technology in hand.

Setup 2: AC simulation (Verifying DC gain, GBW and Phase Margin)

This is the most important setup to validate the gain and stability performance of the proposed design. The simulation setup has been shown in *figure 4.7* and the frequency response curves are plotted in *figure 4.8*, which reveal the Phase Margin (*PM*) compliance to the requirements. The *PM* proves to be very important constrain there as the proposed design consists of two gain stages to achieve the high gain along with higher *PSRR*, there is always a chance of poor stability due to the direct coupling of both gain stages [29, 30]. Hence the pole splitting has been achieved by introduction of the miller capacitance.

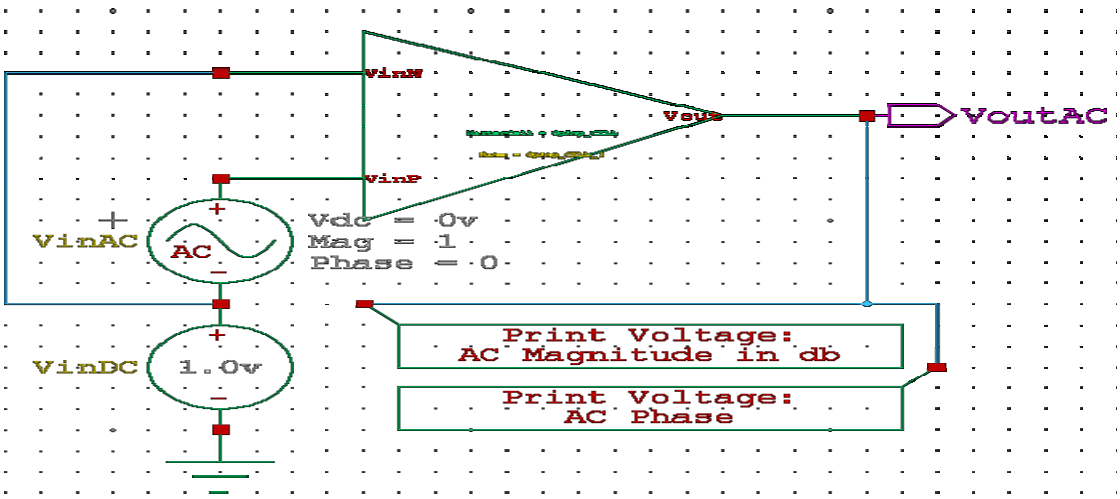


Figure 4.7: AC analysis validation for frequency response (GBW and phase margin)

The achieved parameters are listed as:

Phase Margin achieved: 57^o

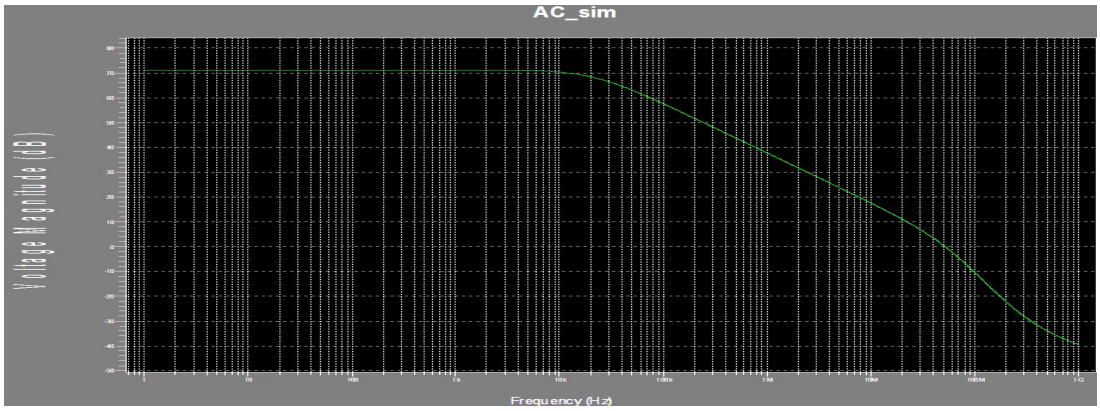
DC gain= 72 DB

GBW= 51 MHz

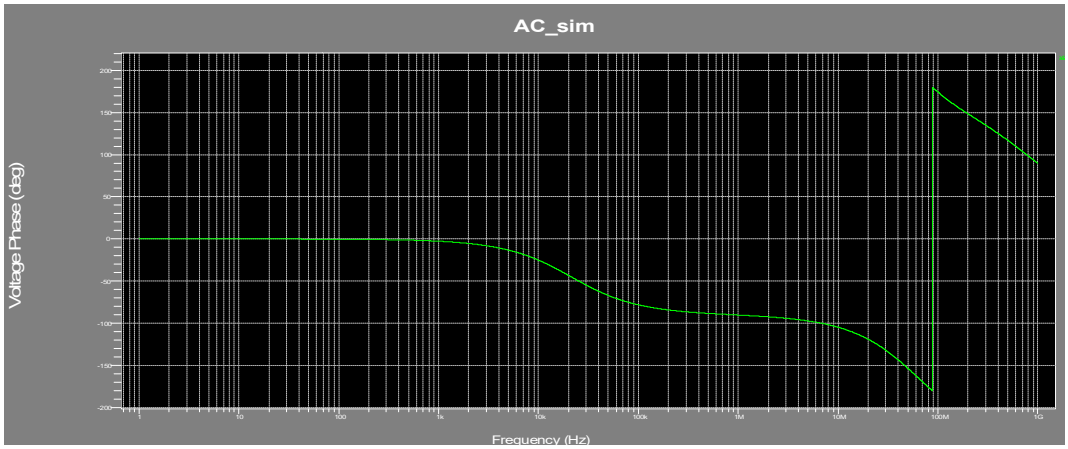
PSRR = -94.66 dB

Setup 3: Transient simulation of Op-Amp in negative feedback (verifying slew rate)

Transient simulation setup (*Figure 4.9*) for any amplifier topology is used to ensure the slew rate and dynamic behaviour. Therefore, it depicts the relative stability and provides an idea to opt for a fair range of *Phase Margin* (generally kept above *30^o - 40^o*) for a faster settlement of the response against any abrupt changes in the input. Therefore, it depicts the relative stability and provides an idea to opt for a fair range of *Phase Margin* (generally kept above *30^o - 40^o*) for a faster settlement of the response against any abrupt changes in the input. But this transient simulation for the slew rate analysis must be carried out in the closed loop (negative feedback) mode of the op amp due to its extremely high open loop gain nature.



(a)



(b)

Figure 4.8: Gain magnitude and Phase (frequency response) of proposed Op-amp (GBW and phase margin)

The transient simulation curves have been plotted in the *figure 4.10*, which depict the performance of the negative feedback op-amp performance against quick variation in the input. One can easily notice a faster settlement of the output with a little ringing character due to the compromised value of the Phase Margin (57^o here). A conventional transconductance based model has been adopted for each of the two stages, to come up with a high gain of *72 dB*, which falls around 4000 on linear scale. The gain bandwidth product on the other hand, comes out to be 51 *MHz*. These values completely satisfy the design targets setup at the onset of the work and the simulated result show that the designed operational amplifier has successfully satisfied all the given specifications.

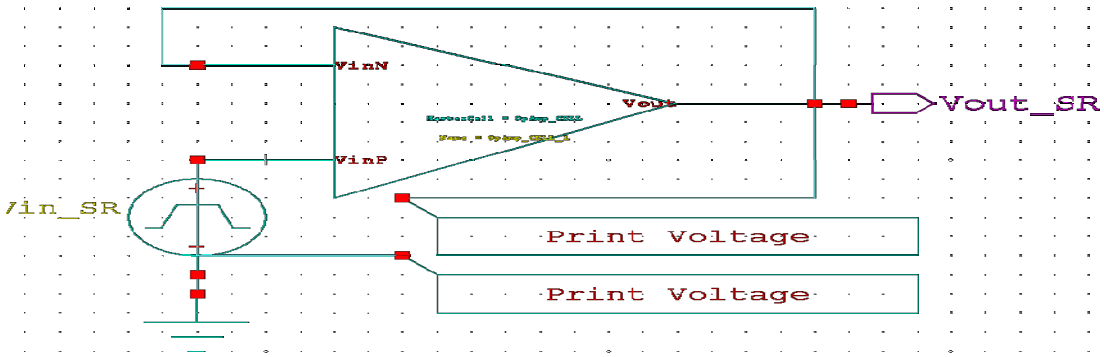


Figure 4.9: Slew rate validation in transient simulation setup (under negative feedback, as voltage buffer)

Measuring slew rate from step response: *SR = 24 V/µs*

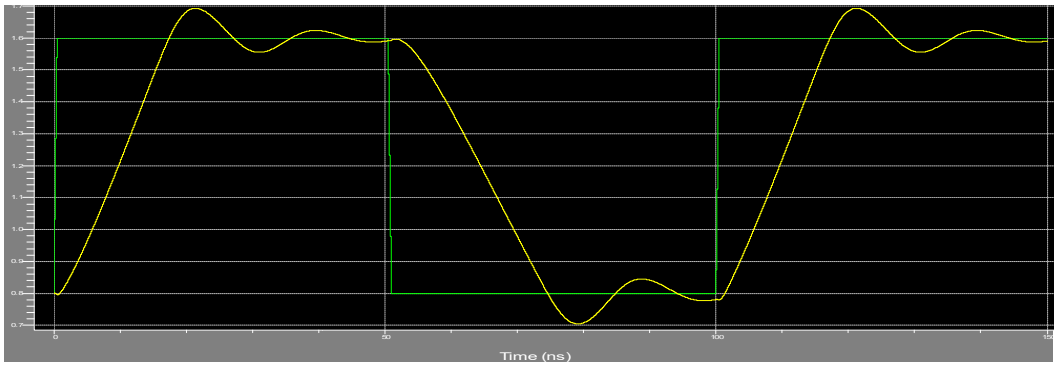


Figure 4.10: Slew rate achieved as targeted, using transient simulation (impact of phase margin ~ 57^{o} is also visible in settlement)

The op amp provides appropriate DC gain and output offset voltage of *23.88 µV* to match the signal to the input range of modern ADC architectures. The operational amplifier has been designed and simulated using *Tanner EDA* (SPICE Platform) in *0.18 µm* (or *180 nm*) *CMOS -1.8 V* process technology. The phase margin achieved is *57o* with the slew rate of *24 V/µs*. The seemingly compromise of the slew rate is all due to the targeted high phase margin which lower the response speed hence slew rate of the amplifier. The designed and implemented two stage operational amplifier also achieved high *PSRR* of *-94.66 dB*, which again promises a remarkable performance in the noisy and supply-fluctuating environment.

CHAPTER 5

FINAL CONCLUSIONS AND FUTURESCOPE

In this dissertation, compensation methods for Op Amps are investigated along with their pros and cons in order for a designer to choose the appropriate scheme for a particular application. This dissertation further explores a creative indirect feedback compensation method which overcomes the major drawback of bandwidth narrowing by the widely used pole-splitting method. It can improve the phase margin as well as extend the bandwidth of the OpAmp. The indirect feedback method can be easily applied to the existing popular two gain stage Op Amp architectures with very little alteration. The mathematical derivation and circuit simulation demonstrate the advanced properties and improved performance of this feed-forward compensation technique.

5.1 Major findings and conclusions

As integrated circuit system are designed to appear as a single-pole system over a wide frequency range to easy the problem that second order and greater system arises regarding stability, compensation techniques must be improved to meet some design specification constrains like higher unity gain frequency and better phase margin.

The indirect feedback technique discussed in this dissertation is a practical and superior compensation scheme for Op Amps, and results in amplifiers with much higher speeds and smaller areas. The design procedure proposed in this dissertation provides simple step by step instructions in designing such an amplifier. The two stage Op Amp designed as a part of this work achieved extremely high performance in comparison to the state of art research works. The amplifier achieved 51 MHz gain bandwidth product while driving a large 1 pF load while using only 30 μA of current. In comparison to the simple miller compensation, the achieved GBW is 10 times larger, and the compensation capacitor is 7

times smaller thus requiring a much smaller area. The Op Amp achieves even two times higher GBW in compared to single stage amplifier with the same total current and total transconductance. Table 5.1 below summarizes the important parameters achieved in the proposed design.

Table 5.1: Achieved parameters of the proposed Two Stage Op-Amp Design

S.No.	**Parameter**	**Typical Value**
1.	DC gain	72 dB ~ 4000
2.	Phase Margin	(PMmin) = 57^{o}
3.	Slew Rate	24 V/μs
4.	Input Common Mode Range	(ICMR+)= 1.6 V
5.	Input Common Mode Range	(ICMR-)= 0.6 V
6.	Power dissipation	$(PD)_{max}$ = 290 μW
7.	Gain Band Width product	(GBW) = 51 MHz
8.	PSRR	-94.66 dB

The overall major performance outcomes of the proposed two-stage miller compensated Op-amp have been listed here, in the Table 5.1, for a quick validation and the appreciation of the novelty of the procedure adopted here.

The presented work here, has proposed and implemented a two stage high gain Op-Amp and has analysed its behaviour in various different simulation environment. A conventional transconductance based model has been adopted for each of the two stages, to come up with a high gain of *72 dB*, which falls around 4000 on linear scale. The gain bandwidth product on the other hand, comes out to be 51 MHz. These values completely satisfy the

design targets setup at the onset of the work and the simulated result show that the designed operational amplifier has successfully satisfied all the given specifications. The op amp provides appropriate DC gain and output offset voltage of *23.88 μV* to match the signal to the input range of modern ADC architectures. The operational amplifier has been designed and simulated using *Tanner EDA* (SPICE Platform) in *0.18 μm* (or *180 nm*) *CMOS -1.8 V* process technology. The phase margin achieved is 57^{o} with the slew rate of *24 V/μs*. The seemingly compromise of the slew rate is all due to the targeted high phase margin which lower the response speed hence slew rate of the amplifier. The designed and implemented two stage operational amplifier also achieved high *PSRR* of *-94.66 dB*, which again promises a remarkable performance in the noisy and supply-fluctuating environment.

5.2 Future Scope and major Amendments

The comparison demonstrated in this dissertation between the Miller compensation technique and the indirect feedback frequency compensation method reflect that this indirect method of compensation reflects potential benefits for providing stability to the operational amplifier. Similarly, this method showed improvement in unity gain frequency and a reduction on the capacitor size. Considering the analysis of this document, indirect feedback compensation shows to be a feasible alternative for compensating amplifiers. Nevertheless, further simulations under specific scenarios should be performed to improve the comparison between these two-compensation techniques.

The future work on this dissertation can be aimed at understanding certain aspects of the circuit and enhancing the characterization of the opamp at cryo temperatures. The following discussion presents an outlook to the possible enhancements to this work.

5.2.1 Circuit-level

Certain aspects of the circuit such as the PSRR, the CMFB action on the CMRR could be further investigated to better understand the circuit. The discrepancy between the measured and simulated values of phase margin and PSRR could be examined in more detail. Simulating the op amp's PSRR by utilizing the EKV model, which incorporates an accurate MOSFET mismatch model, might help in improving the accuracy of PSRR simulations. A study of EKV and the BSIM models could also give more insight into the circuit operation. A revised test setup could be used to characterize the PSRR and CMRR as a function of frequency.

The indirect feedback compensation used in the presented work can be extended to operational amplifier with more than two stages or even different CMOS material processes to explore their advantages against the more commonly used compensation techniques. The technique promises great potential in achieving high speed at low power. As a part of future research the compensation method developed for the two stage amplifier can be extended to realize a three stage and multi-stage amplifiers. A formal derivation and design procedure for multi stage amplifier employing can be developed using the indirect feedback frequency compensation technique. Indirect feedback frequency compensation technique provides a compatible low voltage, low power Op Amp design which can be used to construct high performance data converters, analog filters and other signal processing blocks in the modern sub-micron CMOS process. The technique presented in this dissertation should facilitate the integration of analog circuits in the modern low power high speed applications.

5.2.2 System-level

This work is intended for use in space applications, specifically in lunar missions where the temperature inside lunar craters can go down to −230 °C. Therefore it is essential to investigate the op amp's operation across wide temperature swings ranging from −230 °C

to 120 °C and as well as in radiation intense environments. The test results proved that the circuit is fully functional at −230°C. Although the op amp operates satisfactorily in the desirable temperature range and the degradation effects due to the extreme temperature operation were not noticeable, further verification is needed before assuring the long-term operability of the circuit. The accumulative effects of temperature variation on the lifetime of the devices due to degradation mechanisms such as hot carrier effects, oxide breakdown and carrier freeze out have to be evaluated especially for operations below −180 °C.

REFERENCES

[1] P. R. Gray, and R. G. Meyer, Analysis and design of analog integrated circuits, 3rd ed., New York: Wiley, 1993.

[2] R. J. v. d. Plassche, CMOS integrated analog-to-digital and digital-to-analog converters, 2nd ed., Boston: Kluwer Academic Publishers, 2003.

[3] B. Razavi, Design of analog CMOS integrated circuits, Boston: McGraw-Hill, 2001.

[4] R. J. Widlar, and M. Yamatake, "A Monolothic Power OP AMP," IEEE Journal of Solid-State Circuits, vol. 23, no. 2, pp. 527-535, Apr, 1988.

[5] J. Aguado-Ruiz, A. Lopez-Martin, J. Lopez-Lemus, and J. Ramirez- Angulo, "Power efficient class AB op-amps with high and symmetrical slew rate," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 4, pp. 943–947, Apr. 2014.

[6] M. Figueiredo, R. Santos-Tavares, E. Santin, J. Ferreira, G. Evans, and J. Goes, "A two-stage fully differential inverter-based self-biased CMOS amplifier with high efficiency," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 7, pp. 1591–1603, Jul. 2011.

[7] E. Cabrera-Bernal, S. Pennisi, A. D. Grasso, A. Torralba, and R. G. Carvajal, "0.7-V three-stage class-AB CMOS operational transconductance amplifier," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 11, pp. 1807–1815, Nov. 2016.

[8] T. Stockstad and H. Yoshizawa, "A 0.9-V 0.5 μm rail-to-rail CMOS operational amplifier," IEEE J. Solid-State Circuits, vol. 37, no. 3, pp. 286–292, Mar. 2002.

[9] A. D. Grasso, P. Monsurró, S. Pennisi, G. Scotti, and A. Trifilietti, "Analysis and implementation of a minimum-supply body-biased CMOS differential amplifier cell," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 2, pp. 172–180, Feb. 2009.

[10] P. Monsurró, G. Scotti, A. Trifiletti, and S. Pennisi, “Biasing technique via bulk terminal for minimum supply CMOS amplifiers,” Electron Lett., vol. 41, no. 14, pp. 779–780, Jul. 2005.

[11] J. Ramirez-Angulo and M. Holmes, “Simple technique using local CMFB to enhance slew rate and bandwidth of one-stage CMOS opamps,” Electron. Lett., vol. 38, no. 23, pp. 1409–1411, Nov. 2002.

[12] P. R. Surkanti and P. M. Furth, “Converting a three-stage pseudoclass- AB amplifier to a true-class-AB amplifier,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 59, no. 4, pp. 229–233, Apr. 2012.

[13] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, “Highperformance three-stage single-miller CMOS OTA with no upper limit of CL,” IEEE Trans. Circuits Syst. II, Exp. Brief, to be published, doi: 10.1109/TCSII.2017.2756923.

[14] W. Qu, S. Singh, Y. Lee, Y. S. Son, and G. H. Cho, “Design oriented analysis for miller compensation and its application to multistage amplifier design,” IEEE J. Solid-State Circuits, vol. 52, no. 2, pp. 517–527, Feb. 2017.

[15] M. Tan and W.-H. Ki, “A cascode Miller-compensated three-stage amplifier with local impedance attenuation for optimized complex-pole control,” IEEE J. Solid-State Circuits, vol. 50, no. 2, pp. 440–449, Feb. 2015.

[16] Kavyashree C L, "Design and Implementation of two stage CMOS Operational amplifier using 90nm technology", International Conference on Inventive Systems and Control (ICISC-2017).

[17] G. Shilpa, Nitin Sachdeva, & Tarun Sachdeva. "Analysis and design of a two stage cmos op-amp with 180nm using miller compensation technique." Int. Journal on Recent and Innovation Trends in Computing & Communication (2015): 2255- 2260.

[18] Yang Guanga, Yu Binb, “Design and Analysis of a High-Gain Rail-To-Rail Operational Amplifier,” 2012 International Workshop on Information and Electronics Engineering (IWIEE), ELSEVIER.

[19] Prema Kumar. G, Shravan K Udikala, “Design of Miller Compensated Two-Stage Operational Amplifier for Data Converter Applications,” International Journal of Engineering Research & Technology (IJERT), Vol. 4 Issue 05, May-2015.

[20] Priyanka T, Dr. H S Aravind, Yatheesh Hg, “Design and implementation of two stage operational amplifier,” International Research Journal of Engineering and Technology (IRJET), Volume: 04 Issue: 07, July -2017.

[21] Shirin Pourashraf, Jaime Ramirez-Angulo, Fellow, Antonio J. Lopez-Martin and Ramon González-Carvajal, “A Highly Efficient Composite Class-AB–AB Miller Op-Amp With High Gain and Stable From 15 pF Up To Very Large Capacitive Load,” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, April 18, 2018.

[22] Herve Barthelemy, Remy Vauche, Valentin Gies, Sylvain Bourdel, Jean Gaubert, “Two-stage unbuffered CFOA based non-inverting resistive-feedback amplifier: a study based on the description of the operational transconductance conveyor (OTC),” Analog Integrated Circuits and Signal Processing, SPRINGER 2018.

[23] Bruce Carter and Thomas R.Brown, “Handbook of Operational Amplifer Applications”, Application Report, Texas Instruments, Oct. 2001.

[24] John D. Cressler, “On the Potentials of SiGe HBTs for Extreme Environment Electronics” Proceedings of the IEEE, Vol. 93, No. 9, pp. 1559-1582, Sep. 2005.

[25] TheNASA, Mars Exploration Rover Mission, http://marsrovers.nasa.gov/mission/

[26] A. Lopez-Martin, M. P. Garde, J. M. Algueta, A. Carlos, R. G. Carvajal, and J. Ramirez-Angulo, “Enhanced single-stage folded cascode OTA suitable for large capacitive loads,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 4, pp. 441–445, Apr. 2018.

[27] 16. S. Pourashraf, J. Ramirez-Angulo, A. J. Lopez-Martin, and R. G. Carvajal, “Super class AB OTA without open-loop gain degradation based on dynamic cascode biasing,” Int. J. Circuit Theory Appl., vol. 45, no. 12, pp. 2111–2118, Dec. 2017.

[28] S. Pourashraf et al., “High current efficiency class-AB OTA with high open loop gain and enhanced bandwidth,” IEICE Electron. Exp. Lett., vol. 14, no. 17, Aug. 2017.

[29] Kun Z, Di W, Zhangfa L. A high-performance folded cascode amplifier. In: 2012 International Conference on Computer and Automation Engineering Conference; 15 January 2012; Mumbai, India. pp. 41-44.

[30] Ishak IS, Murad SAZ and Ahmad MF. “Low power folded cascode CMOS operational amplifier with common mode feedback for pipeline ADC” International Integrated Engineering Summit Conference; 1-4 December 2014; Johor, Malaysia. pp. 1-4.

Paper Publication:

Akhtar Saleem Ansari and Mohd. Amir Ansari "Performance Evaluation of Operational Amplifier with High PSRR in 0.18 μm CMOS Technology" in 10th IEEE International Conference on System Modeling & Advancement in Research Trends (SMART) at TMU, Moradabad, held on 10-11 Dec. 2021pp: 618 - 621 DOI: 10.1109/SMART52563.2021.9676329.

ANNEXURE

Proceedings of the SMART–2021, IEEE Conference ID: 52563
10th International Conference on System Modeling & Advancement in Research Trends, 10th–11th December, 2021
Faculty of Engineering & Computing Sciences, Teerthanker Mahaveer University, Moradabad, India

2021 10th International Conference on System Modeling & Advancement in Research Trends (SMART) | 978-1-6654-3970-1/21/$31.00 ©2021 IEEE | DOI: 10.1109/SMART52563.2021.9676329

Performance Evaluation of Operational Amplifier with High PSRR in 0.18 µm CMOS Technology

Akhtar Saleem Ansari[1], Mohd. Amir Ansari[2], Imran Ullah Khan[3*]
[1,2,3]*Department of ECE, Integral University,* Lucknow, India
*E-mail: [1]asansari@student.iul.ac.i, [2]mamir@iul.ac.in, *[3]iukhan@iul.ac.in*

***Abstract*—In this paper the performance evaluation of operational amplifier (Opamp) is carried out in reference to the advantages of high supply rejection in 0.18µm CMOS (complementary metal oxide semiconductor) technology. This evaluation is carried out with Miller Compensation. This process involves nine step procedure in which various parameter such as transconductance, W/L ratio, beta, various current is evaluated. This process is carried out in SPICE platform using Tanner EDA tool. Miller compensation technique is used because with it a reduction in the compensation capacitor size is observed. It further reduces design area and improves the phase margin from the left hand plane zero.**

Keywords- Gain, PSRR, W/L Ratio, CMOS and Miller Compensation.

I. Introduction

An Opamp is fundamentally a 3-terminal device includes inverting, non inverting and output terminals. Inputs of opamp are having very high impedances. Inverting means a (–) sign and non-inverting means (+) sign, shown in Figure 1[1].

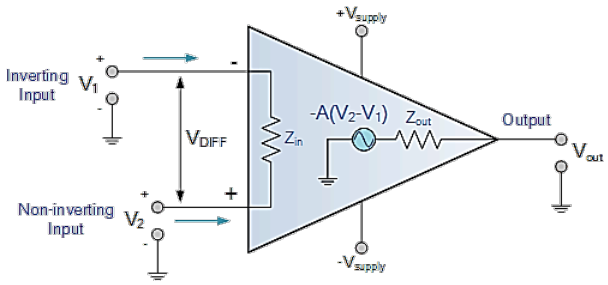


Fig. 1: Opamp Practical Model (2)

Third terminal is the opamp output port either source/ sink, a voltage/current.

In a linear opamp, the output signal is the amplification factor, given as $A \times V_{in}$, where A is amplifier gain and V_{in} is input signal value.

Gain depends on the nature of input and/or output signals. Further Opamp can be classified as.

VIVO represents voltage, VICO represents transconductance, CIVO represents transresistance and CICO represents current.

V stands for voltage, C stands for current, I for Input and O for Output. Important characteristics of Opamp involves [2, 3]

- Voltage Gain-∞
- Input Impedance-∞
- Bandwidth-∞
- Output impedance-0

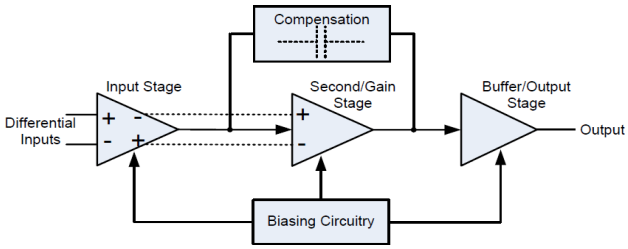


Fig. 2: Opamp basic Model (2)

II. Power Challenges In Opmaap

Temperature increase tends to increase in leakage power in turn increases the total power consumption. Causes thermal runaway under extreme conditions.

$$P_{static} = I_{LEAK} \cdot V_{DD} \quad (1)$$

Where

P_{static} - Static power dissipation,

I_{LEAK} - Sum of the leakage currents of MOSFET (off state)

V_{DD} - Supply Voltage

$$P_{dynamic} = f \cdot C_L \cdot V_{DD}^2 \quad (2)$$

Where

f - Frequency,

C_L - Load Capacitance

To keep power density within the limit supply voltage must be scaled down [4].

Figure 3 shows Octagon analogue design includes;

1. Power Dissipation
2. Supply Voltage
3. Input / Output Impedance
4. Speed
5. Voltage Swing
6. Gain

7. Linearity
8. Noise

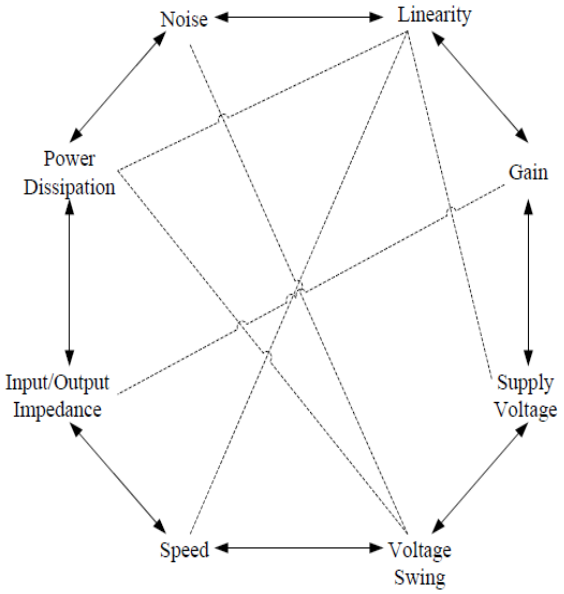


Fig. 3: Analogue Design Octagon

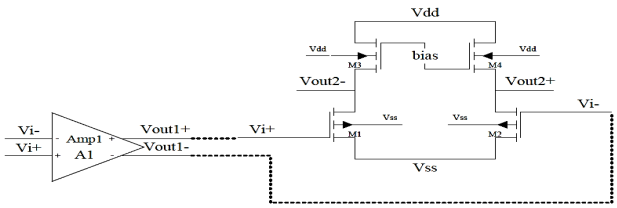


Fig. 4: Two- Stage OpAmp

III. Design Procedure

For High PSRR, miller compensated two stage CMOS op amp (figure 6) are used [5].

Below equations represents MOSFET

1. Strong Inversion [5]
2. Square Law equations [6,7]

Drain Current $I_D = \beta V_{OV}^2 = (\mu_{n,p} C_{OX}/2).(W/L).V_{OV}^2$ (3)

Where $\beta = (\mu_{n,p} C_{OX}/2).(W/L)$

Aspect Ratio $= W/L = 2I_D / (\mu_{n,p} C_{OX}).V_{OV}^2$ (4)

Transconductance $= [(2.\mu_{n,p} C_{OX}).(W/L).I_D]^{1/2}$ (5)

$= 2I_D / V_{OV}$ (6)

Designing involves following nine steps;

STEP 1: Compensation capacitor Cc is evaluated in below manner;

$$C_C > \frac{2.2}{10} \times C_1$$

$$C_C > \frac{2.2}{10} \times 10 \times 10^{-12}$$

$$C_C > 2.2 \times 10^{-12}$$

$$\text{Choose } C_c = 2.2pE \quad (7)$$

STEP 2: Bias current I_5 is evaluated as follows;

Slew rate (SR) $= (I_{SS}/C_c) = (I_5/C_c)$ (8)

Where $I_{SS} = I_5$ is the tail current

$I_5 = SR \times Cc = 50 \times 106 \times 2.3 \times 10^{-12} = 115\ \mu A$

STEP 3: Assuming GB as 120 and transconductance g_{m1} and width to length ratio $(W/L)_{1,2}$ can be find as

$$g_{m1} = GB \times Cc = 2 \times 2.3 \times f \times Cc \quad (9)$$

$$g_{m1} = 120 \times 106 \times 2.3 \times 10^{-12}$$

$$= 0.0017 = 1.7\ m\ \Omega^{-1}$$

$$(W/L)_{1,2} = (g_{m,1})^2/K_n \times I_5 \quad (10)$$

$$= (1.7 \times 10^{-3})^2/(343.2 \times 10^{-6} \times 115 \times 10^{-6})$$

$$= 73.22$$

STEP 4: Design for W/L for M_3 and M_4 from the maximum input voltage specification.

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_5}{K_p \times \left[V_{DD} - V_{inmax} - |V_{tp,3max}| + V_{tn,1min}\right]^2}$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{115 \times 10^{-6}}{70.4 \times 10^{-6} \times [1.65 - 1.3 - 0.42 + 0.42]^2} \quad (11)$$

$$= 14$$

STEP 5: Design for W/L for M5 from the maximum input voltage specification.

$$V_{DSS} = V_{inmin} - V_{SS} - V_{tn,1max} - \sqrt{I_S/\beta_1} \quad (12)$$

$$= 0.1867$$

$$(W/L)_5 = 2I_5 / K_n C_{OX} V_{S5} = 19.22 \quad (13)$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_5}{K_n C_{OX} \times V_{SS}} = 19.22$$

STEP 6: Find g_{m6}, g_{m4} to design W/L of M_6

$$g_{m6} = 10 \times g_{m1} = 10 \times 1.7 \times 10^{-3} = 17\ m\ \Omega^{-1}$$

$$g_{m3} = [v2 \times K_p \times (W/L)_3 \times I_5/2]$$

$$= [v2 \times 70.4 \times 10^{-6} \times 14 \times 115 \times 10^{-6}/2] \quad (14)$$

$$= 0.337\ m\ \Omega^{-1}$$

Let $V_{SG,4} = V_{SG,6}$

$$\text{Therefore, } \left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 \times \frac{g_{m,6}}{g_{m,4}} = 14 \times \frac{17 \times 10^{-3}}{0.337 \times 10^{-3}} = 706.23$$

STEP 7: Calculate I_6 flowing through M_6

$$I_6 = \frac{(g_{m,6})^2}{2 * K_p * \left(\frac{W}{L}\right)_6}$$

$$= \frac{(17 * 10^{-3})^2}{2 * 70.4 * 10^{-6} * 706.23} \quad (15)$$

$$= 2.9\ mA$$

STEP 8: Design W/L for M7 to achieve the desired crrent rations between I_6 and I_5

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5 * \frac{I_6}{I_5}$$

$$= 19.22 * \frac{2.9 * 10^{-3}}{115 * 10^{-6}}$$

$$= 484.67 \quad (16)$$

STEP 9: Design W/L for M_8 by relationship relating to load, compen.

$$(W/L)_8 = (W/L)_6/(1+C_L/C_C) \quad (17)$$

$$= 706.23/(1+ 10\times 10^{-12}/2.3 \times 10^{-12})=132$$

This completes all the design parameter of the proposed Op-amp architecture in figure 6.

IV. Results

To simulated and analyzed the design, TANNEREDA and ADS with 0.18 µm technology is used.

There are three setups for Miller compensated technique used in the two stage operational amplifier in SPICE environment.

1. Opamp Design and DC simulation,
2. AC simulation (Verifying DC gain, GBW and Phase Margin) at
3. Transient simulation of Op-Amp in negative feedback (verifying. In this paper first one is simulated) Simulation setup is shown in figures 5, 6 & 7.

DC simulation performs the following tasks;

1. Verify the common mode range operation
2. Design with targeted ICMR at $ICMR^+$ and $ICMR^-$ = 1.6 V and 0.6 V respectively for all transistors in Saturation

For $ICMR^+$ and $ICMR^-$ equal to G_m = 543 and 483 µmho for M_1 and M_2 & P_D =294 and 280 µW respectively.

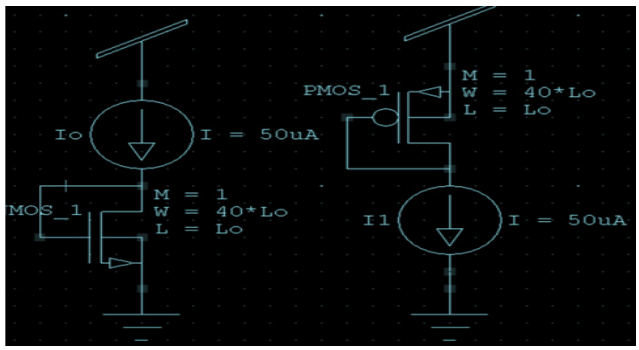


Fig. 5: Experimental Setup

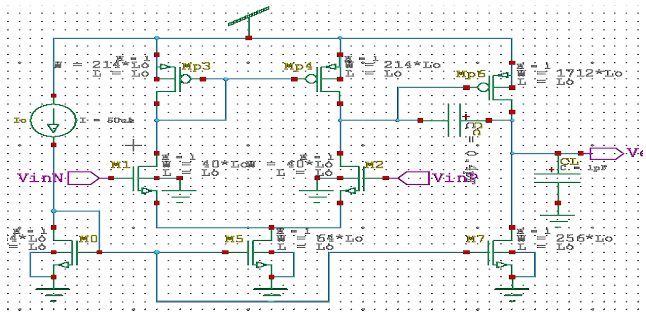


Fig. 6: Two Stage Opamp Based on Miller Compensated Technique (SPICE Environment)

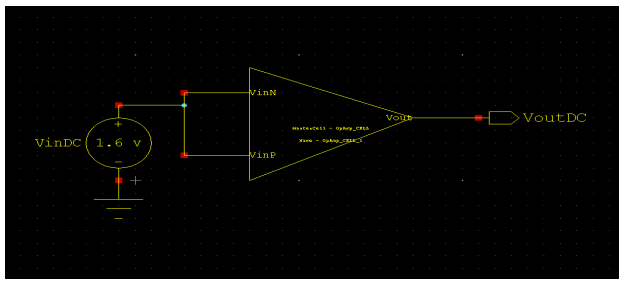
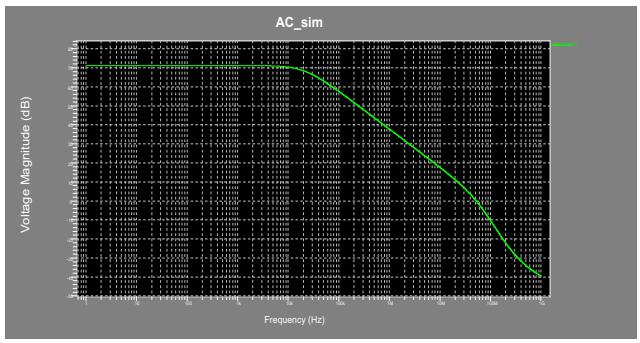


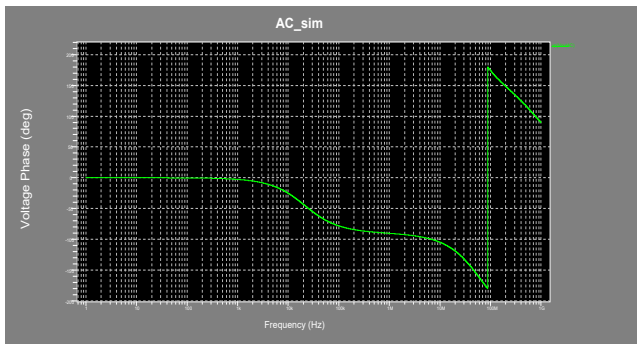
Fig. 7: DC Analysis Validation for ICMR and Gm

Therefore, the G_m for M_1 and M_2 remains 500 µS approximately.

The measured DC power dissipation is 290 µW, well being near to ideal one.



(a)



(b)

Fig. 8: Magnitude and Phase Response of Proposed Op-amp

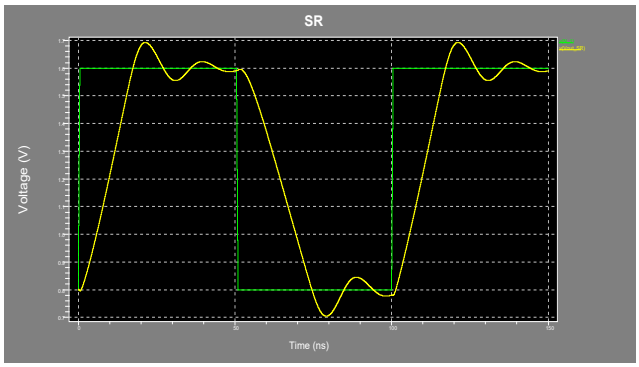


Fig. 9: Achieved Slew Rate

V. Conclusion

The work presented here, has proposed and carried out a two phase high gain Op-Amp and has examined its conduct in different diverse simulation settings. An ordinary model based on transconductance has been taken on for every one of the two phases, to concoct a high increase of 72 dB, on linear scale is found to be 4000. The GBW is of the order of 51 MHz. These qualities totally fulfill the plan targets arrangement at the beginning of the work and the re-enacted result show that the planned functional enhancer has effectively fulfilled. The Opamp has been planned and simulated utilizing Tanner EDA (SPICE Platform) in 0.18 µm technology with CMOS-1.8 V. The achieved values are phase margin 57°, slew rate of 24 V/µs. PSRR obtained is - 94.66 dB.

References

[1] Plassche R. J. V. D., CMOS IC A to D and D to A converters, 2nd edition., Boston: K. Academic Publishers, 2019.

[2] Kavyashree C L, "Design and Implementation of two stage CMOS Operational amplifier using 90nm technology", International Conference on Inventive Systems and Control (ICISC-2017).

[3] Shilpa G., Sachdeva N., & Sachdeva T. "Analysis and design of a two stage cmos op-amp with 0.18 µm using miller compensation technique." Int. Journal on Recent and Innovation Trends in Computing & Communication (2015): 2255- 2260.

[4] Bruce Carter and Thomas R. Brown, "Handbook of Operational Amplifer Applications", Application Report, Texas Instruments, Oct. 2001.

[5] John D. Cressler, "On the Potentials of SiGe HBTs for Extreme Environment Electronics" Proceedings of the IEEE, Vol. 93, No. 9, pp. 1559-1582, Sep. 2005.

[6] Lopez-Martin, M. P. Garde, J. M. Algueta, A. Carlos, R. G. Carvajal, and J. Ramirez-Angulo, "Enhanced single-stage folded cascode OTA suitable for large capacitive loads," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 4, pp. 441–445, Apr. 2018.

[7] S. Pourashraf et al., "High current efficiency class-AB OTA with high open loop gain and enhanced bandwidth," IEICE Electron. Exp. Lett., vol. 14, no. 17, Aug. 2017.