55 Simulation study of small signal common source amplifier using series and parallel networks of like fetes through PSPICE

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Abstract

Common Source FET amplifiers are one of the popular amplifiers used in small-signal amplification of analogue electronics circuits. Study of common source FET amplifier circuit with modifying the various components possibly produce useful results which will be used in enhancing the circuit designs based on applications needs. Frequency response, voltage gain, input impendence, power dissipation of RC coupled FET common source amplifier are studied by using network of FETs connected in series and parallel with PSpice simulation software

Keywords: FET amplifier, small signal amplifiers, basic electronic circuits

Introduction

Leading technology areas like image processing, satellite communication, mobile communication, biomedical imaging, optical fibre communication need amplifiers which amplify the signals received from sensors or transducers for further processing [1–4]. Depending on the industrial application, amplification needed in term of current gain or voltage gain or power gain over the range of frequencies [5]. Input signals could be in the order of milli volts or micro volts, these signals needed to be amplified to a reasonable levels for further processing [6]. FET has less noise and more stable, smaller size and highly efficient compared to BJT. FET amplifiers have advantages like high current gain, high input impedance and low output impedance. Among the FET amplifiers, FET common source amplifier is used mostly in industry due to its wide and popular range of application in electronics. A Common Source FET amplifier provides medium range voltage gain with added feature of high input impedance and inverted amplified signal [7]. The performance of the amplifier is determined with amplifier parameters like bandwidth, current gain, voltage gain, frequency response, input impedance etc. [8]. There have been research studies to improve the performance of the FET amplifiers in terms of bandwidth, gain, frequency response etc. Recent study of water-gated field effect transistor (WG-FET) common source amplifier at 5 Hz frequency increased the gain from 1.65 dB to 8.05 dB and the unity-gain frequency from 10 Hz to 1 kHz [9]. The integrated JEFT offering more than one decade improvement in the output noise level in the low noise

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performance without compromising on JFET amplifier performance greatly benefits analogue applications [10]. A study conducted using FET common source RC coupled amplifier with network of FETs (F_1 to F_{10}) connected in parallel and series. Study includes exploring the model behaviour, characteristics and amplifier action of FET amplifier analysis through PSpice simulation software [6, 11]. The maximum gain changes with increasing number of FETs connected when FETs connected in parallel, for F_1 to F_3 the maximum gain increased from 10.66 to 19.11 [12]. It has been proved that resistors are connected in series or parallel to meet different voltage and current needs of a circuit, FETs can also be connected in parallel or series for a required applications [7, 13, 14]. So, the current study explores the dependence of voltage gain, frequency response, input impedance, total power dissipation and bandwidth on various frequencies for selected amplifier circuits with network of FETs (F_1 to F_{10}) connected in series and parallel using PSpice simulation software [15, 16].

Experimental Setup and Observations

Two different common source FET amplifier configurations shown in Figure 55.1 and 2 are being used and exhaustively study is being carried out about voltage gain, frequency response, total power dissipation, input impedance with respect to frequency.

Figure 55.1 and 55.2 shows the CS amplifier circuits with three identical FETs in parallel and series respectively.

The field effect transistor used here in for the present studies as active element is an n-channel JFET J2N3818. Similarly, Rsr=500Ω, R_1=600KΩ, R_2=110KΩ, R_D=10KΩ, R_S=5KΩ, R_L=10KΩ, C_1=1μF, C_2=1μF and C_S=10μF are used as passive biasing elements in the respective circuits. All the circuits are biased with +15V DC supply voltage V_{CC}. The observations are made for 1V AC signal voltage at 1 KHz frequency (drawn from 1V AC source voltage) through PSpice simulation software [11, 15] student version 9.5.2.

Results and Discussions

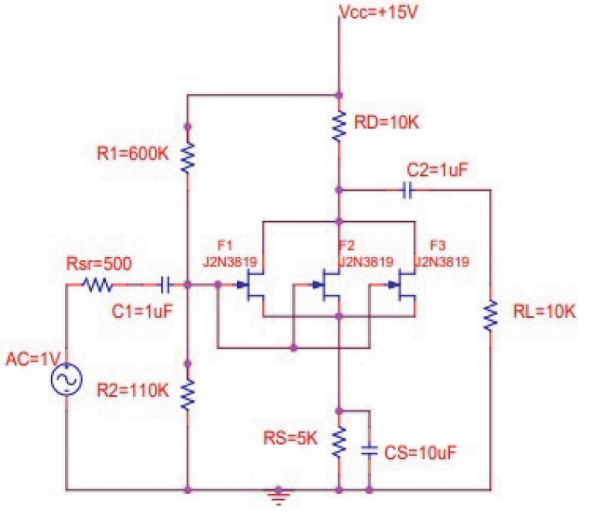

Figure 55.1: JFETs in parallel

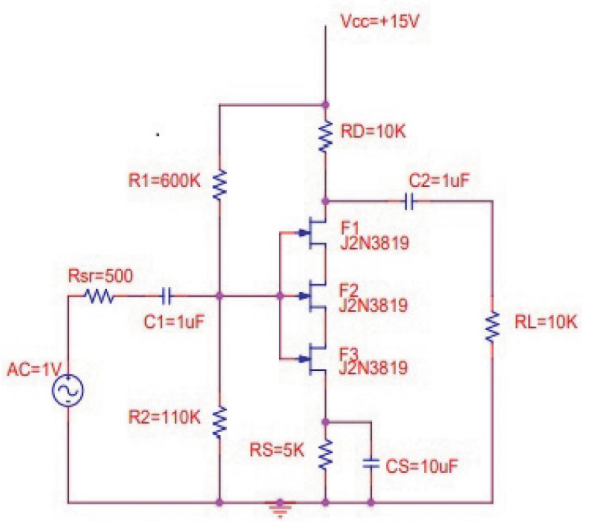

Figure 55.2: JFETs in series

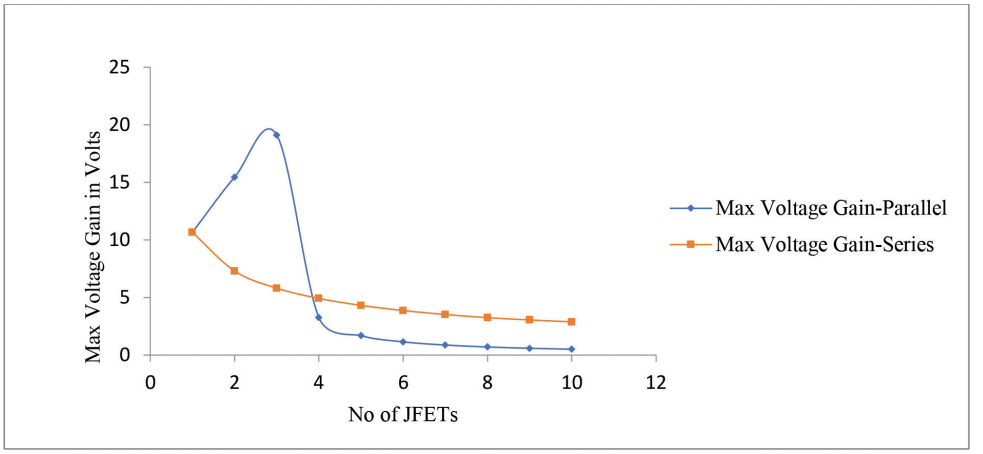

Figure 55.3: Maximum voltage gain with multiple JFETs connected in parallel and series

Figure 55.3 shows the variation of maximum voltage gain over the range of frequencies 1 Hz to 1GHz of input signal applied with number of FETs connected in parallel and series. When FETs connected in parallel the maximum voltage gain increased from 10.66 to 19.11 for F_1 to F_3 then drastically decreased to 3.24 for F_4 then further reduced gradually to 0.5 for F_{10}. At F_7 amplifier demonstrated attenuator behaviour with maximum voltage gain of 0.866. In case of FETs connected in series the maximum voltage gain decreased gradually from 10.66 to 2.88 for F_1 to F_{10}. Table 55.1 has the details.

$$A_V = -(\mu . Vi . R_D) \div [rd + R_D + (\mu+1) R_S]$$

where, $\mu = rd . gm$

Figure 55.4 shows the bandwidth variation of FET amplifier over the range of frequencies 1 Hz to 1GHz of input signal applied with number of FETs connected in

Table 55.1: Table of Maximum Voltage and Bandwidth

No of JFETs	*Maximum Voltage Gain*		*Bandwidth in Hz*	
	Parallel	*Series*	*Parallel*	*Series*
1	10.66	10.66	1.5425E+07	1.5425E+07
2	15.44	7.302	6.1142E+06	1.7337E+07
3	19.11	5.808	3.5249E+06	1.7341E+07
4	3.249	4.917	1.1343E+07	1.6448E+07
5	1.683	4.311	1.3406E+07	1.5141E+07
6	1.142	3.865	1.3378E+07	1.3720E+07
7	0.8655	3.519	1.2747E+07	1.2312E+07
8	0.6975	3.248	1.1969E+07	1.0979E+07
9	0.5844	3.044	1.1195E+07	9.6288E+06
10	0.503	2.882	1.0465E+07	8.4110E+06

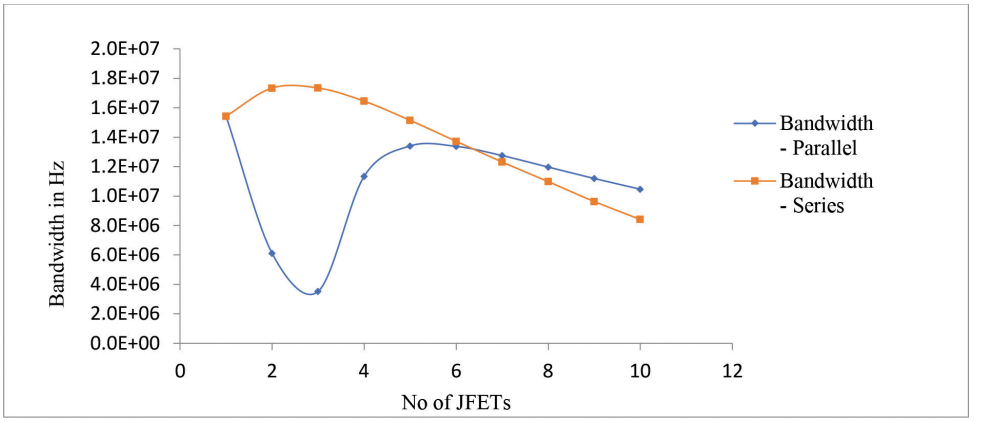

Figure 55.4: Bandwidth with multiple JFETs connected in parallel and series

parallel and series. When FETs connected in parallel the bandwidth decreased from 15.42MHz to 3.52MHz for F_1 to F_3 then drastically increased to 13.40MHz for F_5 then further reduced gradually to 10.46MHz for F_{10}. While FETs connected in series the bandwidth increased from 15.42MHz to 17.34MHz for F_1 to F_3 then decreased gradually to 8.40MHz for F_{10}. Table 55.1 has the details.

Figure 55.5 depicts the variation of FET amplifier input impedance over the range of frequencies 1 Hz to 1GHz of input signal applied with multiple FETs connected in parallel and series. When FETs connected in parallel the input impedance increased from 93.47KΩ to 93.61KΩ for F_1 to F_3 then drastically decreased to 93.47KΩ for F_4 then further reduced gradually to 93.32KΩ for F_{10}. While network of FETs connected in series the input impedance decreased from 93.47KΩ to 93.33KΩ for F_1 to F_{10}. Table 55.2 has the details.

Figure 55.6 shows the total power dissipation variation of FET amplifier over the range of frequencies 1 Hz to 1GHz of input signal applied with network of FETs connected in parallel and series. When FETs connected in parallel the total power dissipation increased from 1.38×10^{-02} watts to 1.52×10^{-02} watts for F_1 to F_{10} due to increase in I_D for multiple JFETs. While FETs connected in series the total power

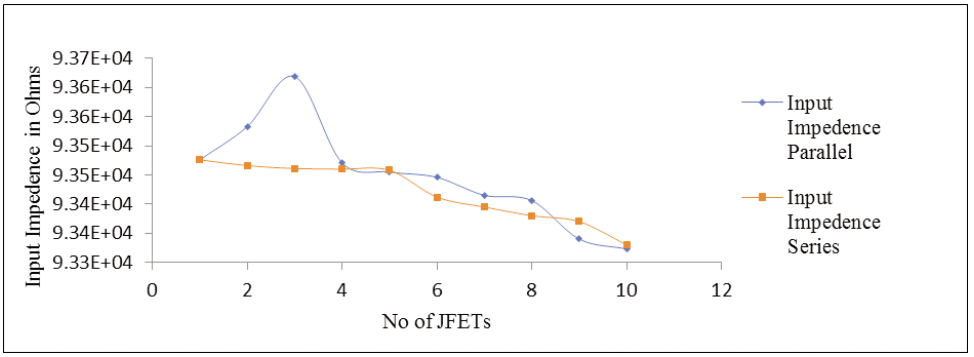

Figure 55.5: Input impedance when multiple JFETs connected in parallel and series

Table 55.2: Input Impedance and Total Power Distribution

No of JFETs	*Input Impedance in Ω*		*Total Power Dissipation in Watts*	
	Parallel	*Series*	*Parallel*	*Series*
1	9.35E+04	9.35E+04	1.38E-02	1.38E-02
2	9.35E+04	9.35E+04	1.45E-02	1.29E-02
3	9.36E+04	9.35E+04	1.48E-02	1.22E-02
4	9.35E+04	9.35E+04	1.50E-02	1.17E-02
5	9.35E+04	9.35E+04	1.50E-02	1.13E-02
6	9.34E+04	9.34E+04	1.51E-02	1.09E-02
7	9.34E+04	9.34E+04	1.51E-02	1.05E-02
8	9.34E+04	9.34E+04	1.52E-02	1.02E-02
9	9.33E+04	9.34E+04	1.52E-02	9.95E-03
10	9.33E+04	9.33E+04	1.52E-02	9.70E-03

dissipation decreased from 1.38×10^{-02} watts to 9.70×10^{-03} watts for F_1 to F_{10} due to decrease in I_D. Table 55.2 has the details.

Figure 55.7 depicts the frequency response of FET amplifier over the range of frequencies 1 Hz to 1GHz of input signal applied with network of FETs connected in parallel. When FETs connected in parallel the maximum voltage gain increased from 10.66 to 19.11 for F_1 to F_3 then drastically decreased to 3.24 for F_4 then further reduced gradually to 0.5 for F_{10}. At F_7 amplifier demonstrated attenuator behaviour with maximum voltage gain of 0.866. In case of FETs connected in series the maximum voltage gain decreased gradually from 10.66 to 2.88 for F_1 to F_{10}.

Figures 55.8 and 55.9 depicts the frequency response of FET amplifier over the range of frequencies 1 Hz to 1GHz of input signal applied with network of FETs connected in series. In case of FETs connected in series the maximum voltage gain decreased gradually from 10.66 to 2.88 for F_1 to F_{10}.

Figure 55.10 shown the Drain, Gate and Source voltages of FET amplifier with network of FETs connected in parallel and series. In case of FETs connected in series the drain voltage increased gradually from 6.01V to 8.74V for F_1 to F_{10}. No change in gate voltage. Source voltage decrease from 4.49V to 3.12V for F_1 to F_{10}. When FETs connected in parallel the drain voltage decreased gradually from 6.01V to 5.08V for

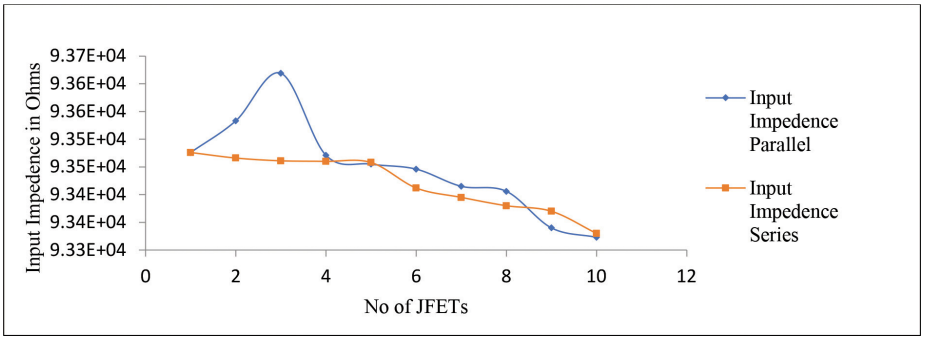

Figure 55.6: Total power dissipation when multiple JFETs connected in parallel and series

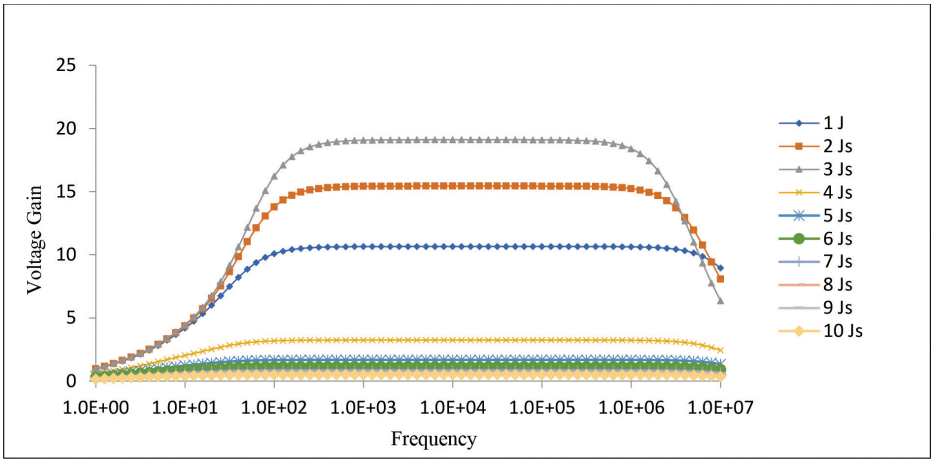

Figure 55.7: Frequency response of JFET amplifier with multiple JFETs connected in parallel

F_1 to F_{10}. No change in gate voltage. Source voltage increased from 4.49V to 4.95V for F_1 to F_{10}

Conclusions

Maximum voltage gain increases with increasing number of FETs in parallel up to three FETs from 10.66 to 19.11. Maximum voltage gain rapidly decreased for four FETs in parallel to 3.24 then maximum voltage gain gradually decreases to 0.50 for ten FETs. In case of FETs in series, maximum voltage gain decreases from 10.66 to 2.88 for ten FETs. When FETs connected in parallel the bandwidth decreased from 15.42MHz to 3.52MHz for F_1 to F_3 then drastically increased to 13.40MHz for F_5 then further reduced gradually to 10.46MHz for F_{10}. While FETs connected in series the bandwidth increased from 15.42MHz to 17.34MHz for F_1 to F_3 then decreased gradually to 8.40MHz for F_{10}. When FETs connected in parallel the input impedance increased from 93.47KΩ to 93.61KΩ for F_1 to F_3 then drastically decreased to 93.47KΩ for F_4 then further reduced gradually to 93.32KΩ for F_{10}. While network of FETs connected in series the input impedance decreased from 93.47KΩ to 93.33KΩ

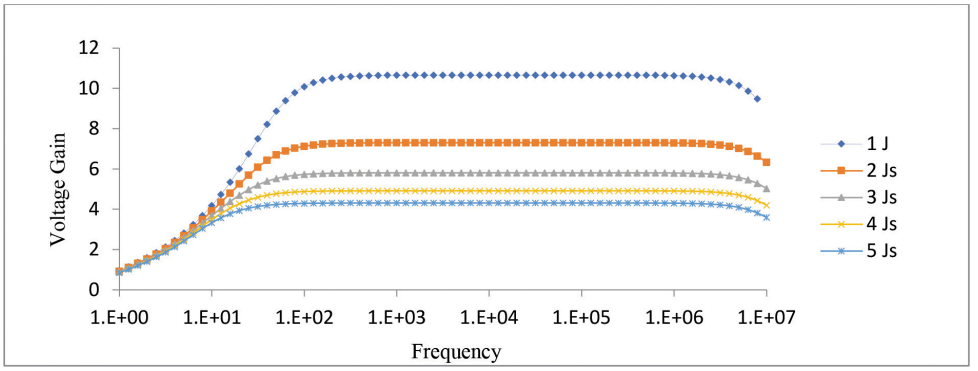

Figure 55.8: Frequency response of FET amplifier with multiple JFETs connected in series F_1 to F_5

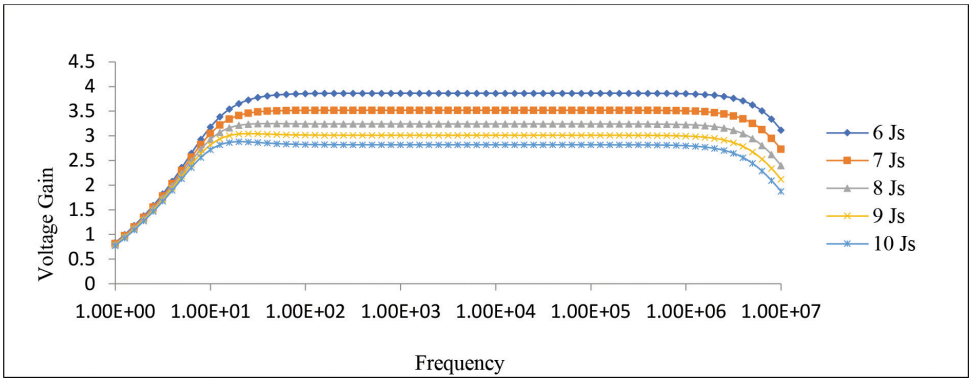

Figure 55.9: Frequency response of FET amplifier with multiple JFETs connected in series F_6 to F_{10}

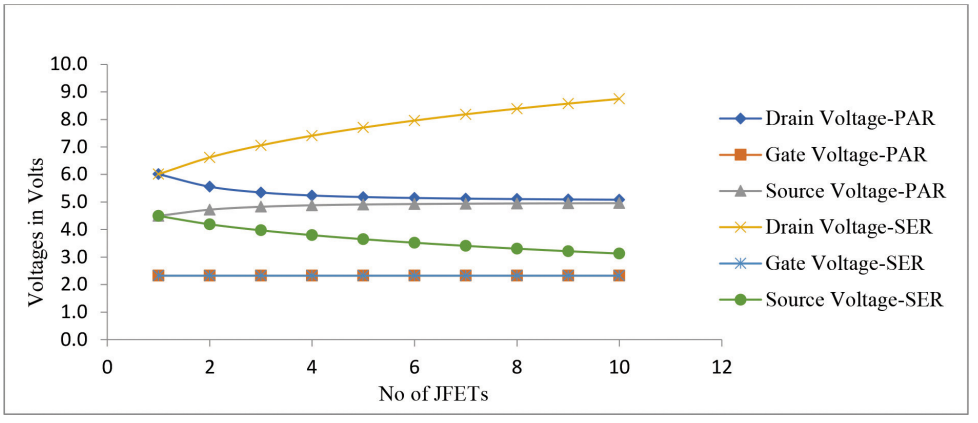

Figure 55.10: JFET terminal voltages when multiple JFETs connected in parallel and series

for F_1 to F_{10}. The total power dissipation increases as number FETs increases in parallel. The total power dissipation decreases with increasing number of FETs in series. Voltage gains of selected FET amplifiers are less than that of BJT (under similar configuration) amplifiers but current gains are comparatively larger [17].

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